



DESIGN AND DEVELOPMENT OF A BACKEND FOR AN **ULTRA-FAST** **SENSOR** READING SYSTEM



Dr. Ing Alan Ezequiel Fuster



Dr. Ing Iván Peric



INTRODUCTION

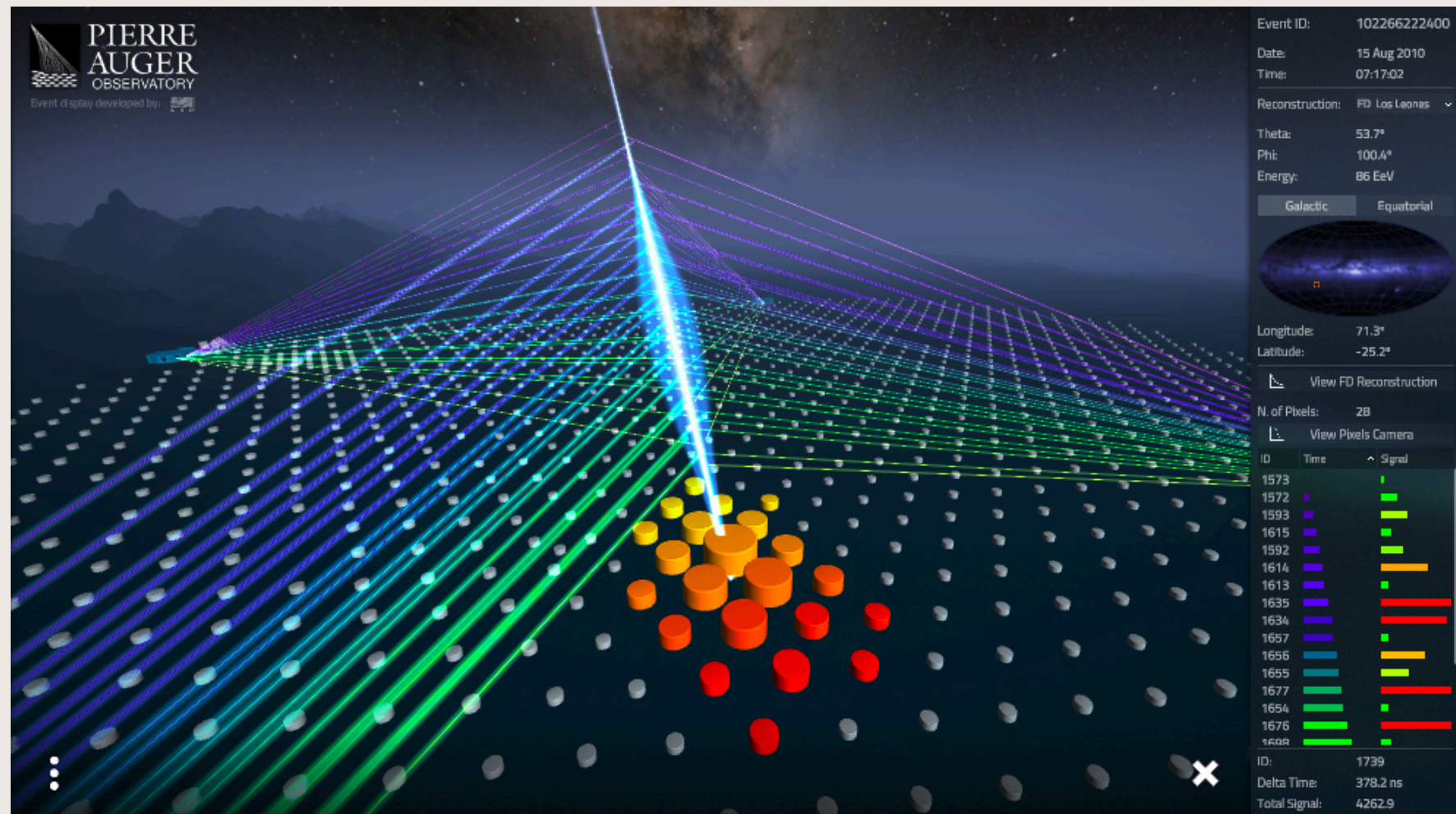
ORDER OF THE PRESENTATION:

1. CONTEXT

2. STAGES OF THE CURRENT DESIGN

3. SUBJECTS

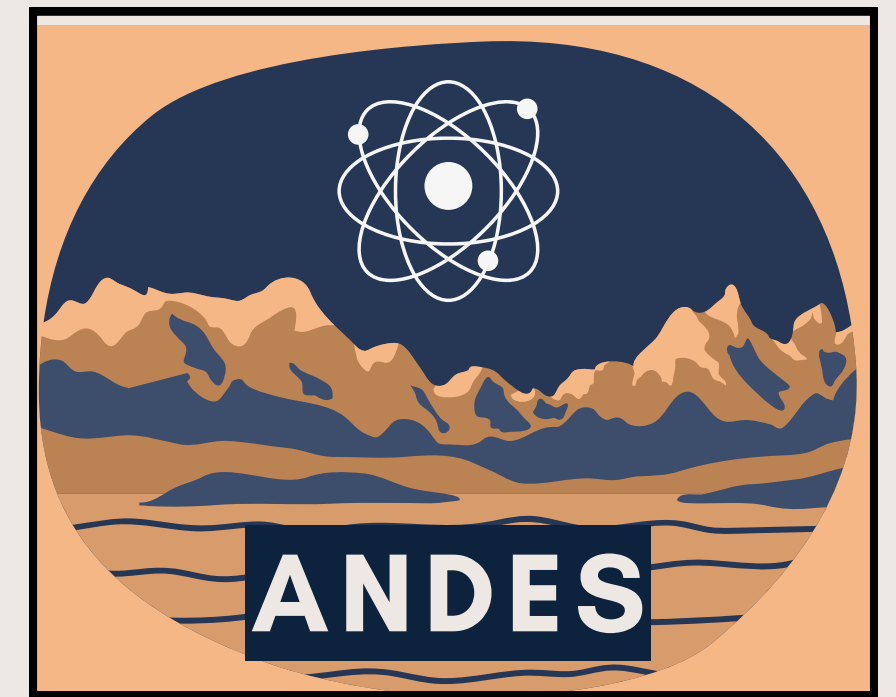
CONTEXT



The Pierre Auger Observatory detects cosmic rays indirectly by observing the particle showers they create when colliding with the atmosphere. It uses two complementary techniques: a network of over 1,600 surface detectors (water tanks that record Cherenkov light produced by passing particles) and fluorescence telescopes that capture the faint light emitted by excited air molecules during the shower's development. This combination allows precise reconstruction of the cosmic rays' energy and incoming direction.



CONTEXT



The ANDES Underground Laboratory is being planned and designed to be one of the largest and most shielded laboratories in the Southern Hemisphere, which will be located in the Andes Range, in the area of the current Paso Agua Negra that connects the provinces of San Juan (Argentina) and Elqui (Chile).

The diversity of experiments that are being planned, including experiments for the direct and indirect search of dark matter and neutrino precision physics, requires a precise knowledge of the flux of high-energy atmospheric muons within the laboratory.

SPECIFIC OBJECTIVES

In the context of these two major projects, the specific objective of this Thesis Plan **is the design, development, and calibration of a new readout electronics system for photon detection in scintillation modules for both types of muon detectors mentioned above.** In particular, the work focuses on **the synchronization, data acquisition, and storage system (digital Back-End), employing one or more customized Application-Specific Integrated Circuits (ASICs) specifically designed for this application.**

STAGES

OF THE READOUT OF ULTRA HIGH SPEED SENSORS

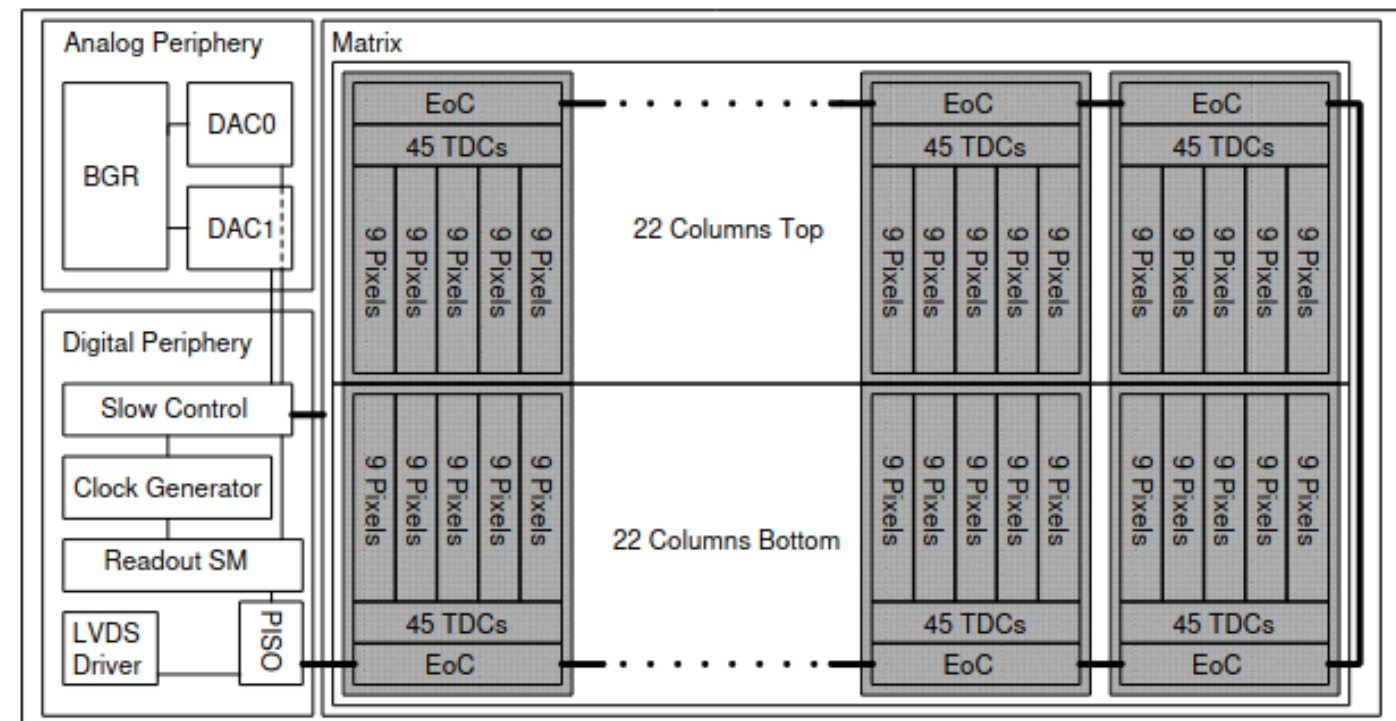
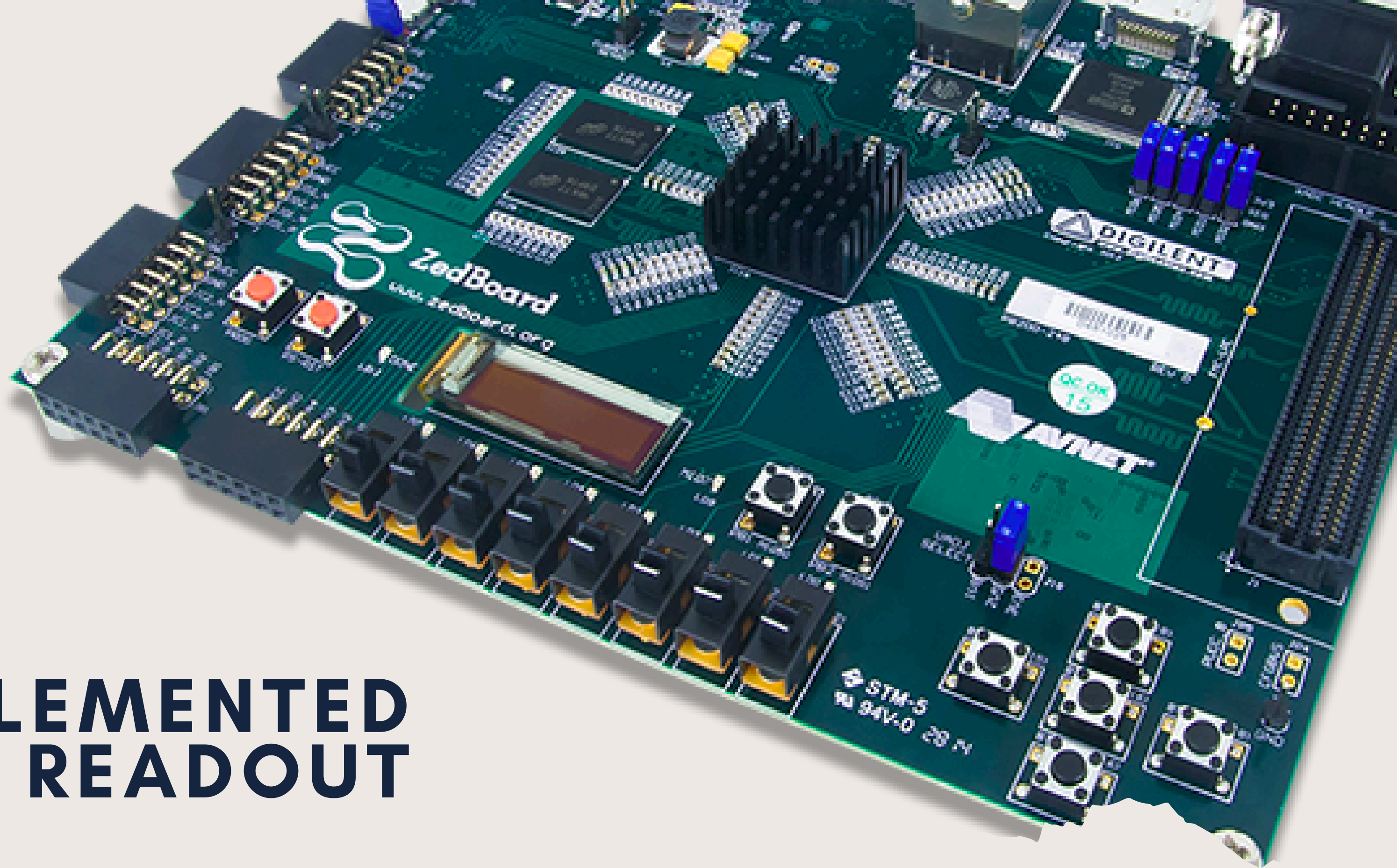


Figure 6: Basic Schematic of Top Level of ANDESPix

Postprocessing MODULE

1. COMMUNICATION UPDATE
2. CLOCK SYNCHRONIZATION LINE.



**IMPLEMENTED
DESIGN READOUT**

ACQUISITION SYSTEM REQUIREMENTS

FUNCTIONAL REQUIREMENTS

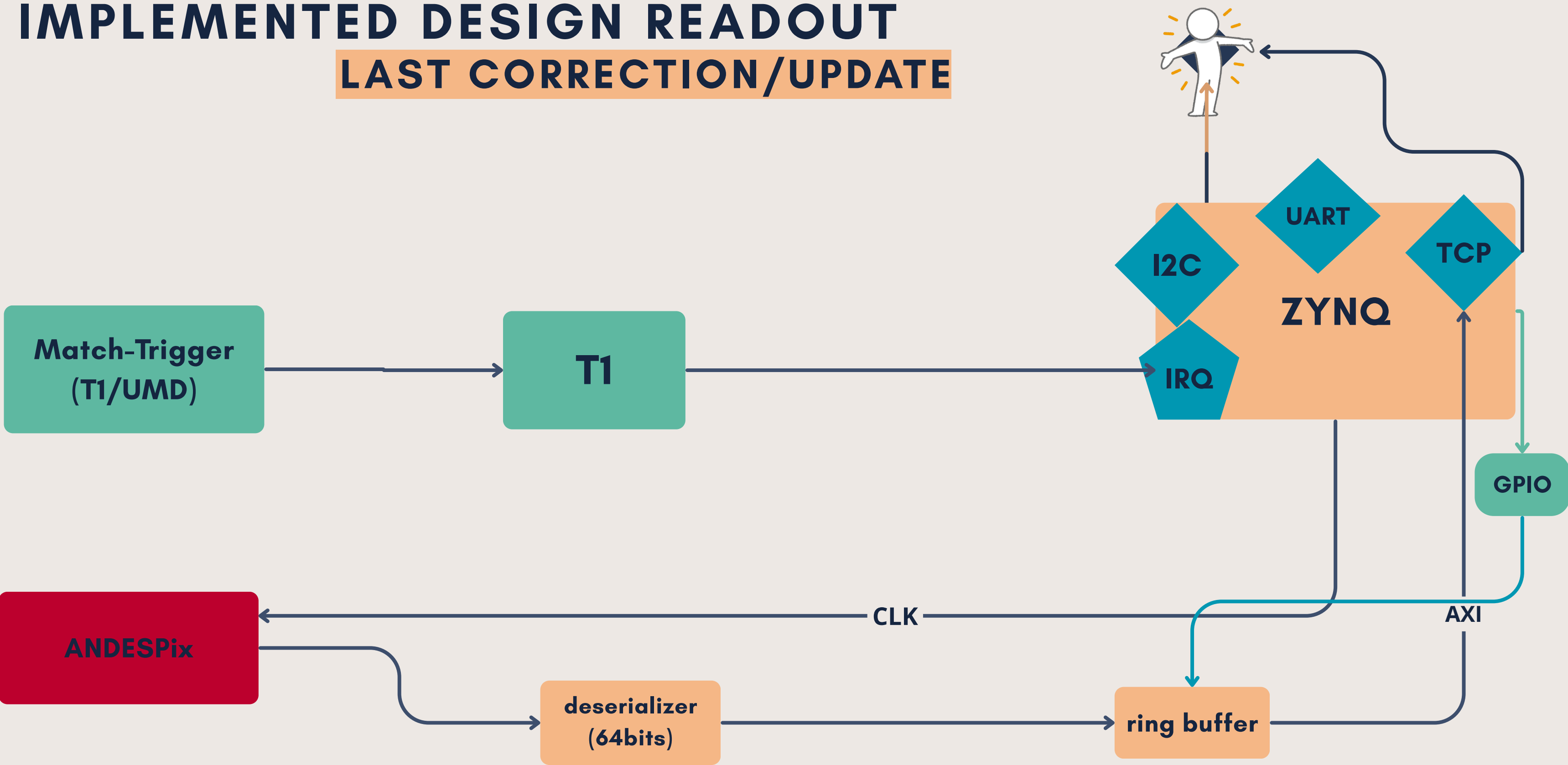
1. Convert LVDS signals to single-ended.
2. Deserialize incoming data into 64-bit words.
3. Store data using DMA channels.
4. Add headers and format data streams.
5. Transmit data over TCP/IP to a remote client.
6. Provide a UART and TCP-based menu for system and chip configuration.
7. Configure the chip via I²C through the TCA6416 expander.
8. Display configuration bus values for verification.
9. Allow independent reset of internal modules.
10. Capture event-triggered data windows (512 samples before and after the trigger) with a second DMA for offline analysis.

NON-FUNCTIONAL REQUIREMENTS

1. Support input data rates up to 160 MHz without data loss.
2. Ensure reliable TCP/IP transmission with data integrity.
3. Provide clear and user-friendly UART interface.
4. Guarantee safe reset of modules without affecting others.
5. Maintain consistent 64-bit word formatting across acquisition, transmission, and decoding.

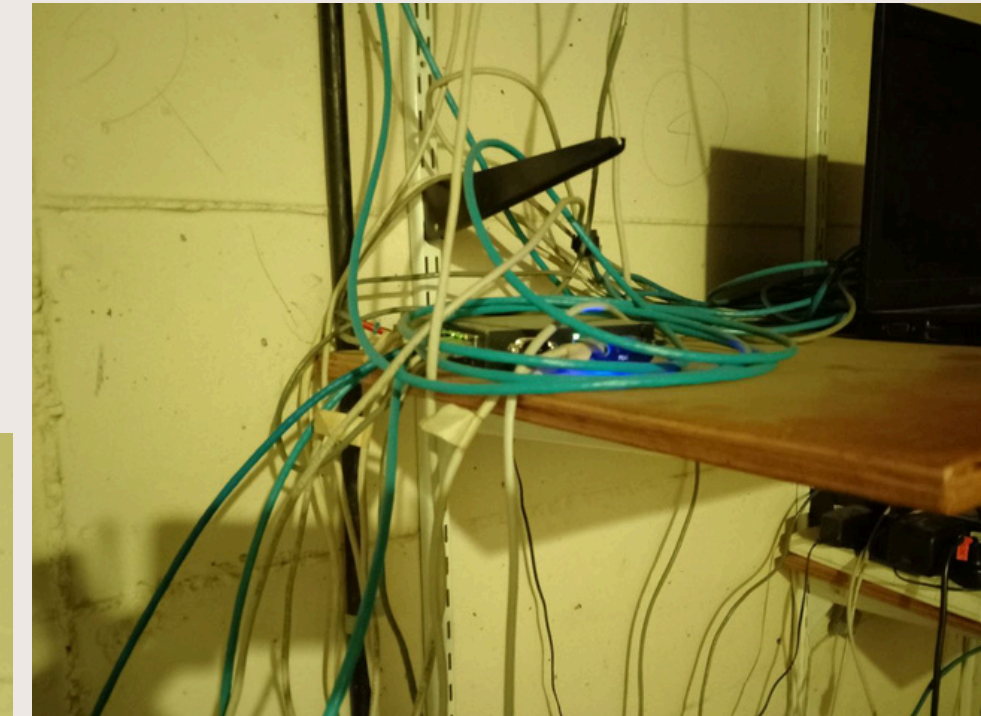
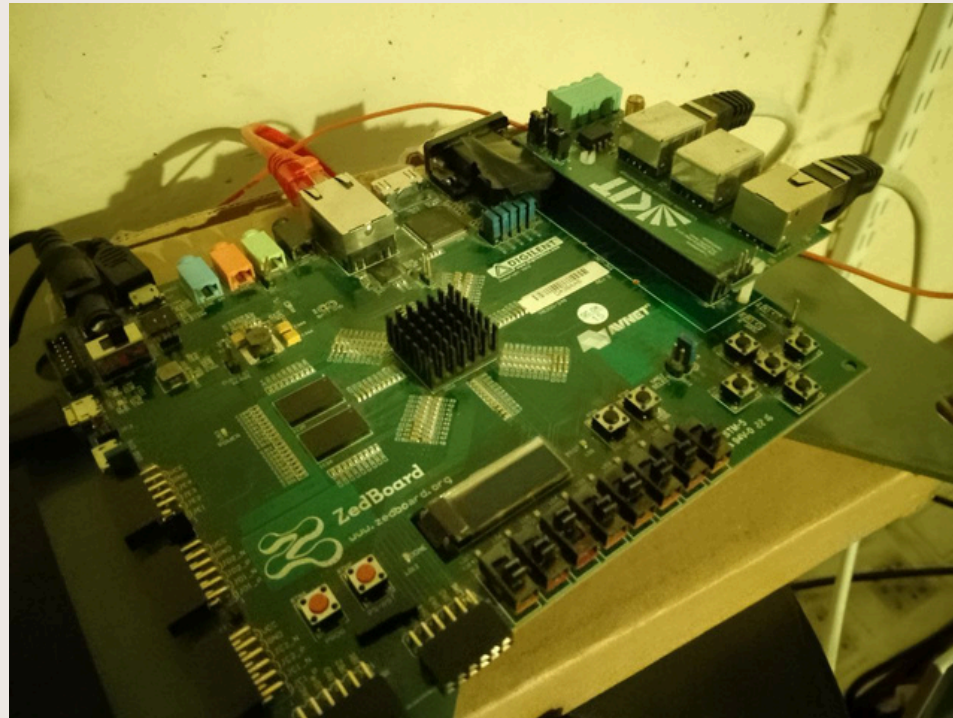
IMPLEMENTED DESIGN READOUT

LAST CORRECTION/UPDATE



IMPLEMENTED DESIGN READOUT

LAST CORRECTION/UPDATE



MUON
COINCIDENCE
DETECTOR
PHOTO IN HD
(PUT HERE)

POST-PROCESSING REQUIREMENTS

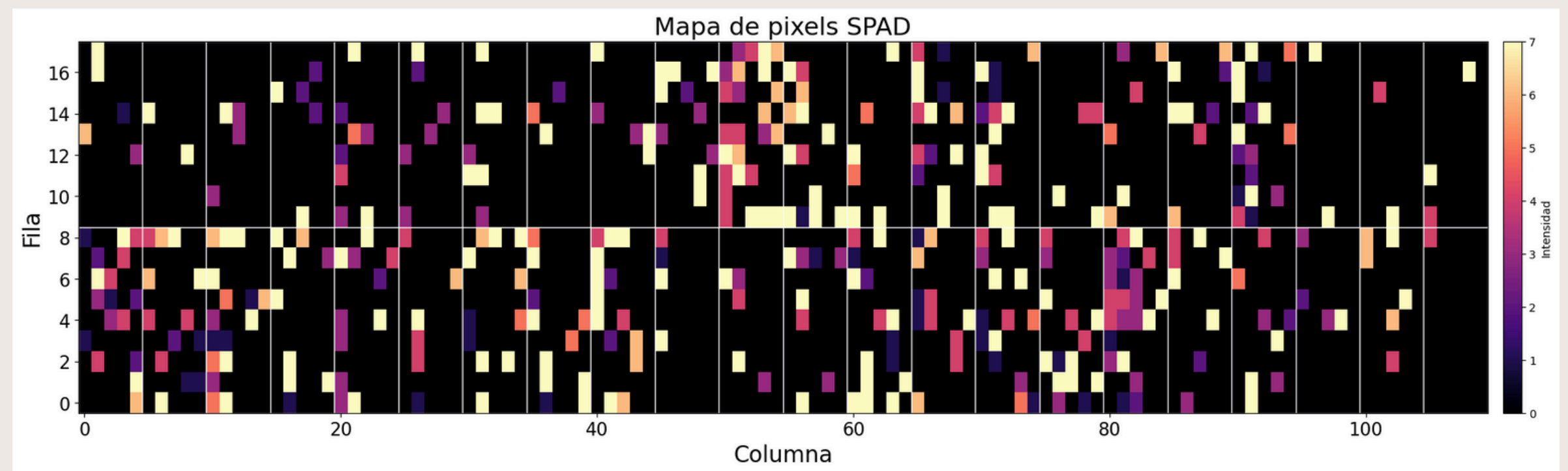
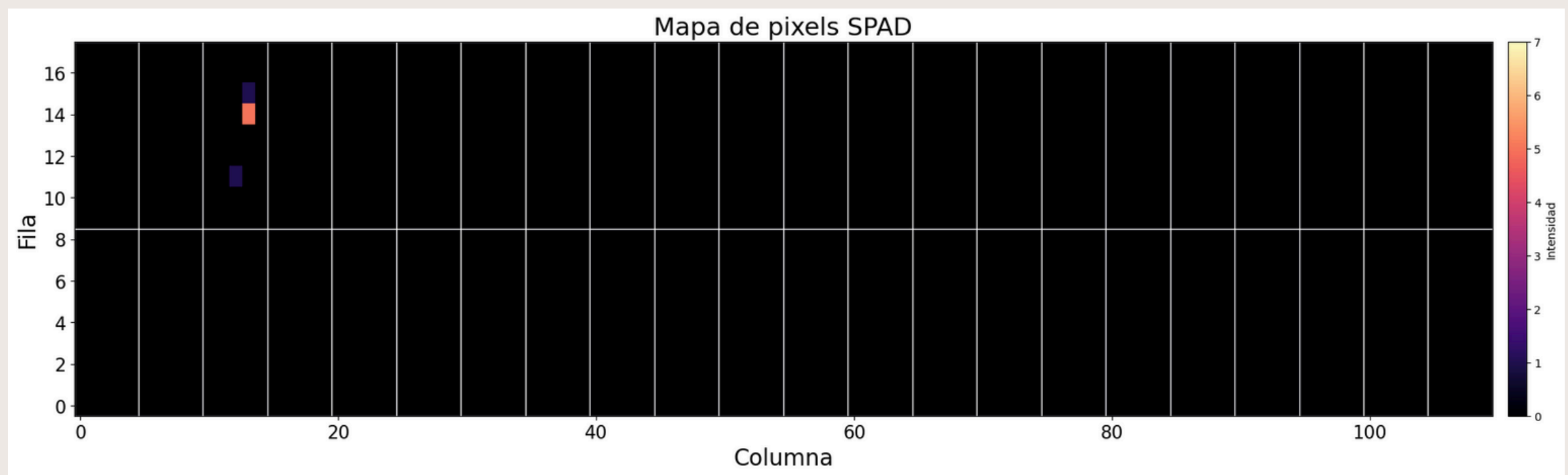
FUNCTIONAL REQUIREMENTS

1. Receive raw data files in .bin (Hexadecimal format) from the Zynq system.
2. Decode binary data into pixel matrix format (rows × columns) according to the addressing scheme defined by the acquisition system.
3. Reconstruct image frames from the decoded pixel matrix.
4. Analyze pixel intensity values across the frame.
5. Identify and mark pixels related to detected events of interest.
6. Store processed and annotated data into a structured database for later retrieval and analysis.

NON-FUNCTIONAL REQUIREMENTS

1. Ensure decoding is fully compatible with the Zynq data output format.
2. The matrix reconstruction must preserve spatial alignment (row/column consistency).
3. Post-processing must handle large data files efficiently (scalability).
4. The database must support queries for event-based retrieval.
5. Ensure reproducibility: same .bin input must always generate the same decoded and processed output.

IMAGES ACQUIRED FROM CURRENT SETUP



SUBJECTS

ADVANCED DIGITAL DESIGN

The main objective of this work is to design and implement a lightweight convolutional neural network (CNN) optimized for real-time image classification, whose filter-polynomial-like structure allows deployment on any digital system, from low-cost FPGAs to SoMs, SoCs, and ASICs

Dr. Eng. Ariel Pola

Telecommunications engineer and PhD in Engineering from the Universidad Nacional del Sur, with expertise in high-speed communications, microelectronics, and advanced signal processing. He has contributed to academic, industrial, and space technology projects, and currently works as a radio ASIC system designer at Ericsson, developing components for 5G mmWave platforms.



PRESENTED AT

Real-Time Detection of Gravitational Waves Using a Fixed-Point Classification Neural Net on Cora Z7

Fernanda Zapata Bascuñán
Escuela de Ciencia y Tecnología
Universidad Nacional de San Martín
Buenos Aires, Argentina
fzapatabascuna@unsam.edu.ar

Alan Ezequiel Fuster
Facultad Regional Buenos Aires
Universidad Tecnológica Nacional
Buenos Aires, Argentina
alan.fuster@iteda.gob.ar

Abstract—Since current neural network development systems in Xilinx and VLSI require co-development with Python libraries, the first stage of a convolutional network has been implemented by developing a convolutional layer entirely in Verilog. We analyze the limitations of numerical representations and compare our implemented architecture, smallnet, with its computer-based counterpart.

I. INTRODUCTION

With the advancement of image processing technologies and the growing integration of control systems, a new paradigm has emerged—one that increasingly relies on processing large volumes of image data for both training and inference. This shift has underscored the need for efficient algorithm implementations, especially as hardware platforms become more accessible and ubiquitous.

The rapid rise of machine learning, particularly deep learning techniques, has further accelerated innovation in image processing. However, deploying these algorithms on embedded systems remains a significant challenge due to their high computational and memory demands [1]. Most existing implementations rely on high-performance, power-intensive hardware, which makes them accessible primarily to well-funded institutions or organizations, and limits their applicability in resource-constrained or cost-sensitive environments.

In this context, the present focuses on designing a lightweight convolutional neural network entirely hand-coded in Verilog, deployable on low-cost FPGAs and free of IP cores. Unlike solutions that rely on pre-built IP cores or high-level libraries, each functional block in this design is developed from scratch, with an optimized pipeline that achieves a significant speedup compared to CPU execution. These characteristics enable the deployment of neural networks in embedded, low-budget environments—where CPU- or GPU-based alternatives are impractical due to cost and energy constraints—or serve as a first step toward ASIC implementation.

The main objective of this work is to design and implement a lightweight convolutional neural network (CNN) optimized for real-time image classification, whose filter-polynomial-like structure allows deployment on any digital system, from low-cost FPGAs to SoMs, SoCs, and ASICs.

As goals and tasks toward the main objective, we consider:

- To reduce computational complexity by simplifying the network architecture, leveraging techniques such as max pooling to downsample feature maps and decrease processing overhead.
- To optimize hardware resource usage to ensure compatibility with resource-constrained, low-power FPGA devices while maintaining acceptable levels of classification accuracy.
- To demonstrate real-time performance by implementing and validating the design in a practical embedded environment.
- To promote accessibility by providing a cost-effective solution suitable for deployment in environments with limited computational or financial resources.

II. BACKGROUND

A CNN is a type of deep neural network composed of cascaded convolutional layers, pooling layers, and fully connected layers. During the feed-forward phase, each convolutional layer applies a set of kernel functions—weight matrices of dimension $k \times k$ —which slide over the input image with a certain stride. Each kernel convolves with a corresponding $k \times k$ window of the input to produce one pixel in the subsequent feature map. This operation extracts spatially localized features by applying learned filters across the input [2]. Pooling layers perform downsampling by aggregating values within a receptive field into a single output, effectively reducing the spatial dimension of the feature maps. Similar to convolutional layers, the pooling window shifts across the input by a stride value. This process enhances spatial invariance by combining features and disregarding minor distortions or shifts in the input data. Moreover, pooling reduces the dimensionality and computational complexity for subsequent

CORA Z7

DIGILENT

PRINCIPLES AND APPLICATIONS OF THE MONTE CARLO METHOD

In this work, we explore the latent space of a denoising variational autoencoder with a mixture-of-Gaussians prior (VAE-MoG). To evaluate how well the model captures the underlying structure, we use Hamiltonian Monte Carlo to draw posterior samples conditioned on clean inputs, and compare them to the encoder's outputs from noisy data.

Dr. Gustavo
Santa Cruz

Physicist with a PhD from the University of Buenos Aires, specializing in nuclear science and its applications to health. At the National Atomic Energy Commission (CNEA), he leads research and international collaborations in advanced cancer therapies, including BNCT and proton therapy.



Dan Beninson
Instituto de Tecnología Nuclear

CASE

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ARGENTINE
CONGRESS OF
EMBEDDED
SYSTEMS

Looks good on the surface? HMC uncovers what the encoder gets wrong.

On the Shape of Latent Variables in a VAE-MoG: A Posterior Sampling-Based Study

Fernanda Zapata Bascuñán
fzapatabascuna@unsam.edu.ar

Abstract

In this work, we explore the latent space of a denoising variational autoencoder with a mixture-of-Gaussians prior (VAE-MoG). To evaluate how well the model captures the underlying structure, we use Hamiltonian Monte Carlo to draw posterior samples conditioned on clean inputs, and compare them to the encoder's outputs from noisy data.

Methods

To evaluate the encoder's denoising capability in latent space, we formulated the following hypothesis: latent codes obtained from noisy inputs (z_{noisy}) should approximate the distribution of those derived from clean data (z_{clean}). To test this, we:

[h0] Fit a Bayesian Gaussian Mixture Model (BGMM) to z_{clean} , representing the reference posterior.

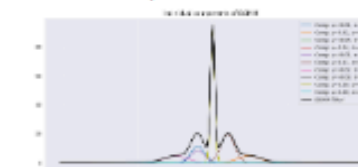


Figure 1. Loss function, KL loss and total training loss of the denoising Convolutional VAE training.

[h1] Sampled from the BGMM using Hamiltonian Monte Carlo (HMC) to

obtain high-quality z_{clean} samples.

[h2] Conducted two-sample Kolmogorov-Smirnov (KS) tests on each latent dimension $d \in \{1, \dots, D\}$.

[h3] Assumed weak inter-dimensional dependencies, allowing marginal comparisons as a proxy for joint alignment.

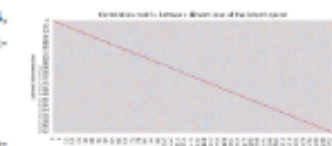


Figure 2. Pearson correlation matrix between latent dimensions z extracted by the encoder. Most correlations are close to zero, suggesting relative independence between dimensions.

Since marginal KS tests assume weak dependence between dimensions, we assessed pairwise correlations to verify this condition. As shown in the figure below, the correlations are low, supporting the reliability of the marginal testing strategy.

Results

The consistently high KS statistics indicate significant differences between the two distributions, as illustrated in figures above. These findings reveal a systematic discrepancy between the encoder's outputs and the true posterior, suggesting that despite visually accurate

reconstructions, the latent space structure is not preserved in the presence of noise.

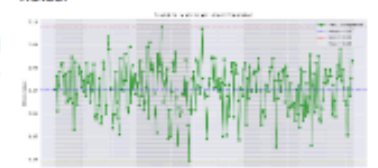


Figure 3. Acceptance rates per latent dimension during HMC sampling, reflecting the proportion of Hamiltonian proposals accepted under the Metropolis criteria.

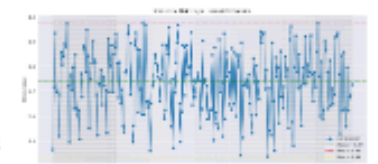


Figure 4. Kolmogorov-Smirnov (KS) statistics across all 256 latent dimensions, shown a significant mismatch between the encoder's latent representations and posterior samples obtained via HMC.

Future Work

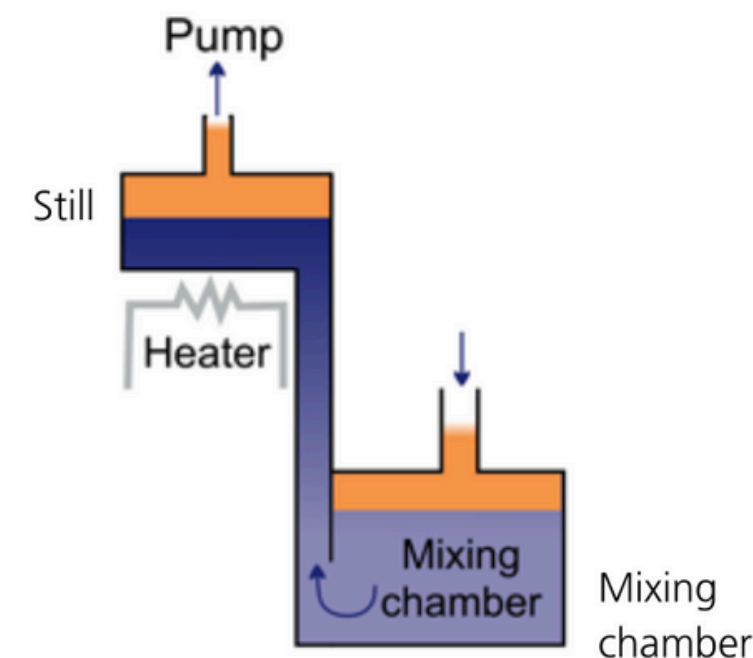
The current BGMM prior also fails to capture key structural features. To address this, we propose exploring flexible priors (e.g., normalizing flows), applying latent regularization techniques like MMD or adversarial penalties, pruning unstable dimensions, and refining the decoder architecture.

UNSAM

CASE

DYNAMIC SYSTEMS AND ARTIFICIAL INTELLIGENCE APPLIED TO DATA MODELING

CONGRESS
YET TO
CHECK...

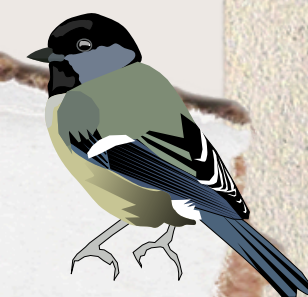


FINAL WORK PROPOSAL:

CHARACTERIZATION OF CRYOGENICS REFRIGERATOR FROM CLASSICAL DESCRIPTION TO SINDY/KAN

Dr. Gabriel Mindlin

Physicist with a PhD from Drexel University, recognized for his contributions to nonlinear dynamics and complex systems, and a recipient of the Arthur Taylor Winfree Award and the 2023 Konex Diploma of Merit. He is a Full Professor at the University of Buenos Aires and a Senior Researcher at CONICET.

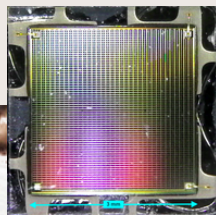


universidad de buenos aires - exactas
departamento de Física

We model and analyze a cryogenic refrigerator using both physics-based and data-driven approaches. Thermal parameters are first identified from experimental step responses through least-squares fitting. Then, Sparse Identification of Nonlinear Dynamics (SINDy) and Kernel Adaptive Networks (KAN) are applied to capture nonlinear behavior directly from data. This hybrid framework links physical insight with data-driven modeling, enabling accurate and interpretable system characterization.

CMOS INTEGRATED CIRCUIT DESIGN

The objective of the course is for students to acquire the knowledge and skills necessary to design a CMOS integrated circuit using a commercial technology. Throughout the course, students carry out a project in which they must plan, design, simulate, and verify a CMOS chip. By the end of the course, students are expected to be capable of undertaking the design of application-specific integrated circuits (ASICs) for research projects, their doctoral theses, or as a tool for innovative technological developments.



Dr. Mariano Garcia-Inza

PhD in Engineering, as well as a degree in Electronic Engineering. His research spans microelectronics, solid-state physics, and the study of ionizing radiation effects on semiconductor devices, with a particular focus on the physics and behavior of MOSFET and CMOS technologies for integrated circuit design and optimization.

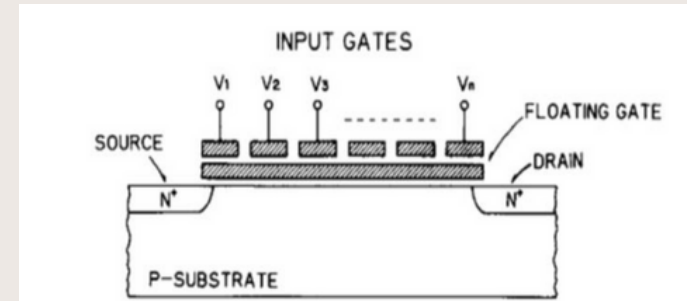


Fig. 1(a) Basic structure of neuron MOS transistor [1-2]

SYNTHESIS, MODELING, ANALYSIS AND SIMULATION METHODS, AND APPLICATIONS TO CIRCUIT DESIGN

PROPOSED CONGRESS



cadence

FINAL WORK PROPOSAL:

COMPARATIVE DEVELOPMENT OF XOR GATE IN NEURON CMOS TECHNOLOGY

This work presents a comparative development of XOR logic gates implemented using neuron CMOS technology. The study evaluates design strategies, performance metrics, and potential advantages in terms of power efficiency, speed, and area compared to conventional CMOS implementations.