Front-end Readout ASIC Design for Ultra-Fast Sensors used in Muon Detectors

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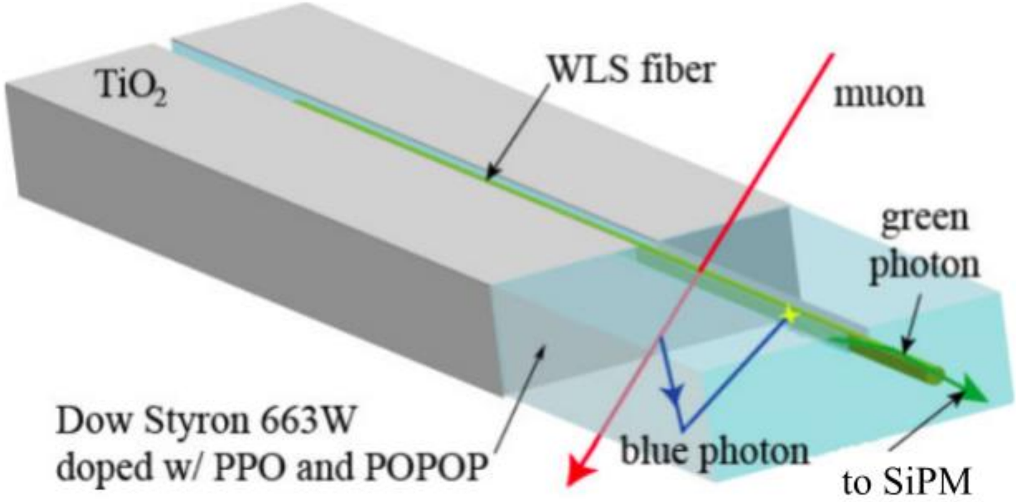
Content

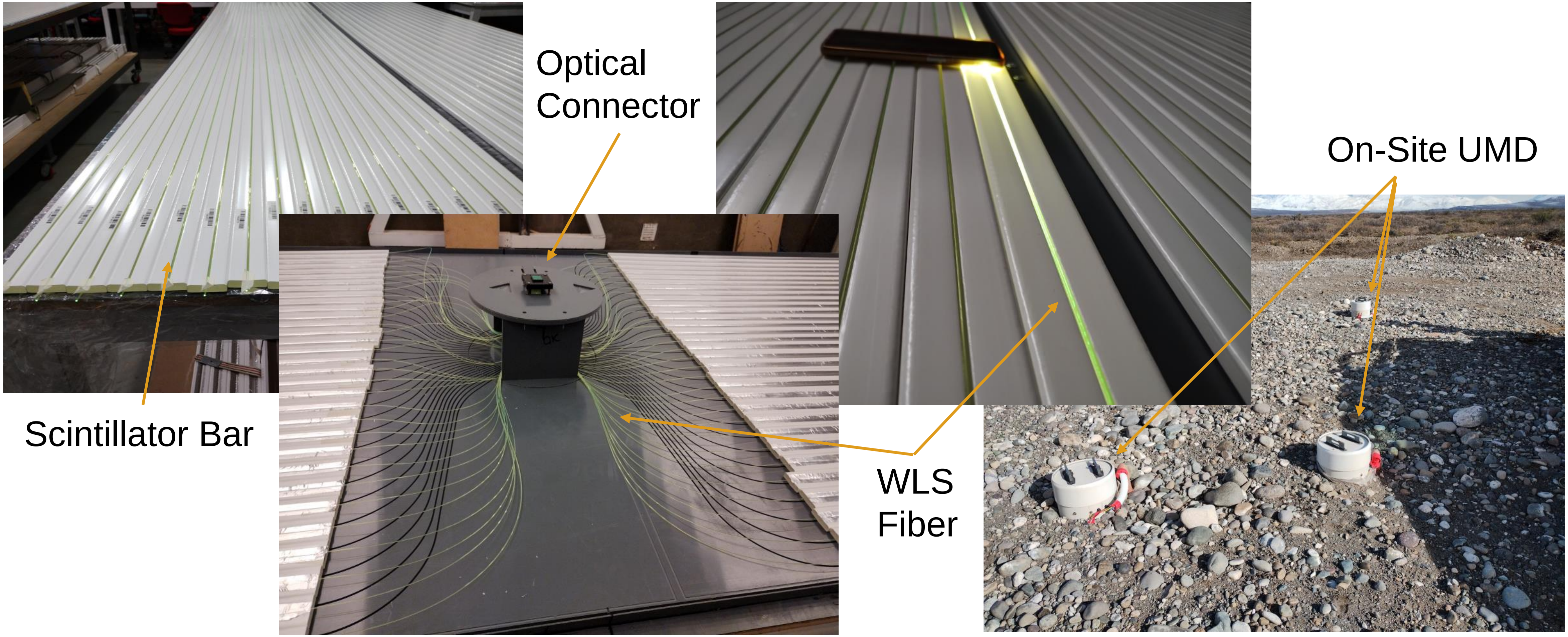
Scintillator Based Muon Detection (e.g. for Muon-Veto in ANDES)



- Muon generates blue photons in scintillator
- Those photons are absorbed by Wavelength Shifting (WLS) Fiber
- SiPM detects green photons emitted by WLS Fiber

Picture adapted from: M. Platino et al., “AMIGA at the Auger Observatory: the scintillator module testing system,” J. Inst., vol. 6, no. 06, pp. P06006–P06006, Jun. 2011, doi: 10.1088/1748-0221/6/06/P06006.

AMIGA Detector Assembly in Malargüe



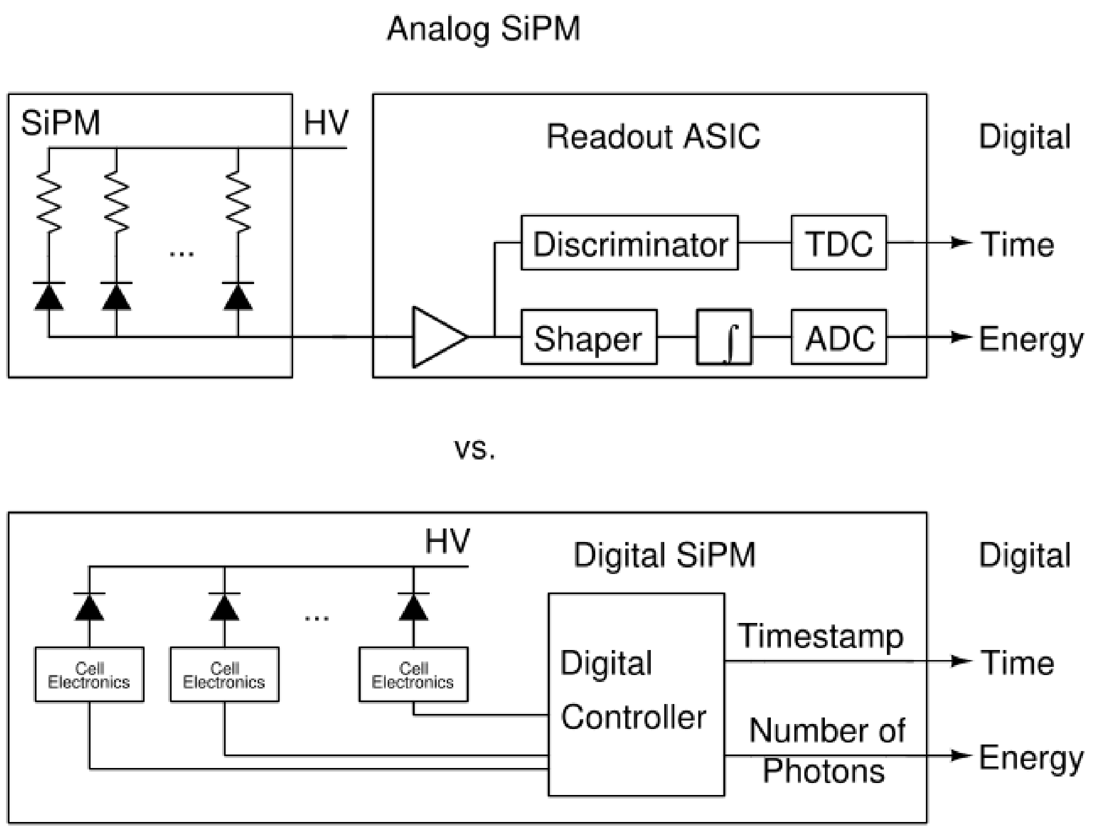
Thanks to Nicolás Leal, Gustavo Ríos, Gabriel Morales, Agustin Morales, Maximiliano Maciel, Luciana Torres and Nicolás Sepúlveda for the detailed introduction to the detector assembly.

Analog vs. Digital SiPM

- SiPM is an array of Single Photon Avalanche Diodes (SPADs)
- Analog SiPM
  - All SPADs in parallel
  - Signal very small when only one SPAD fires
- Digital SiPM
  - Every SPAD has its own readout
  - Large Signal from firing SPAD
  - Noisy SPADs can be masked

→Development of ANDESPix in collaboration KIT-ITeDA-CAB

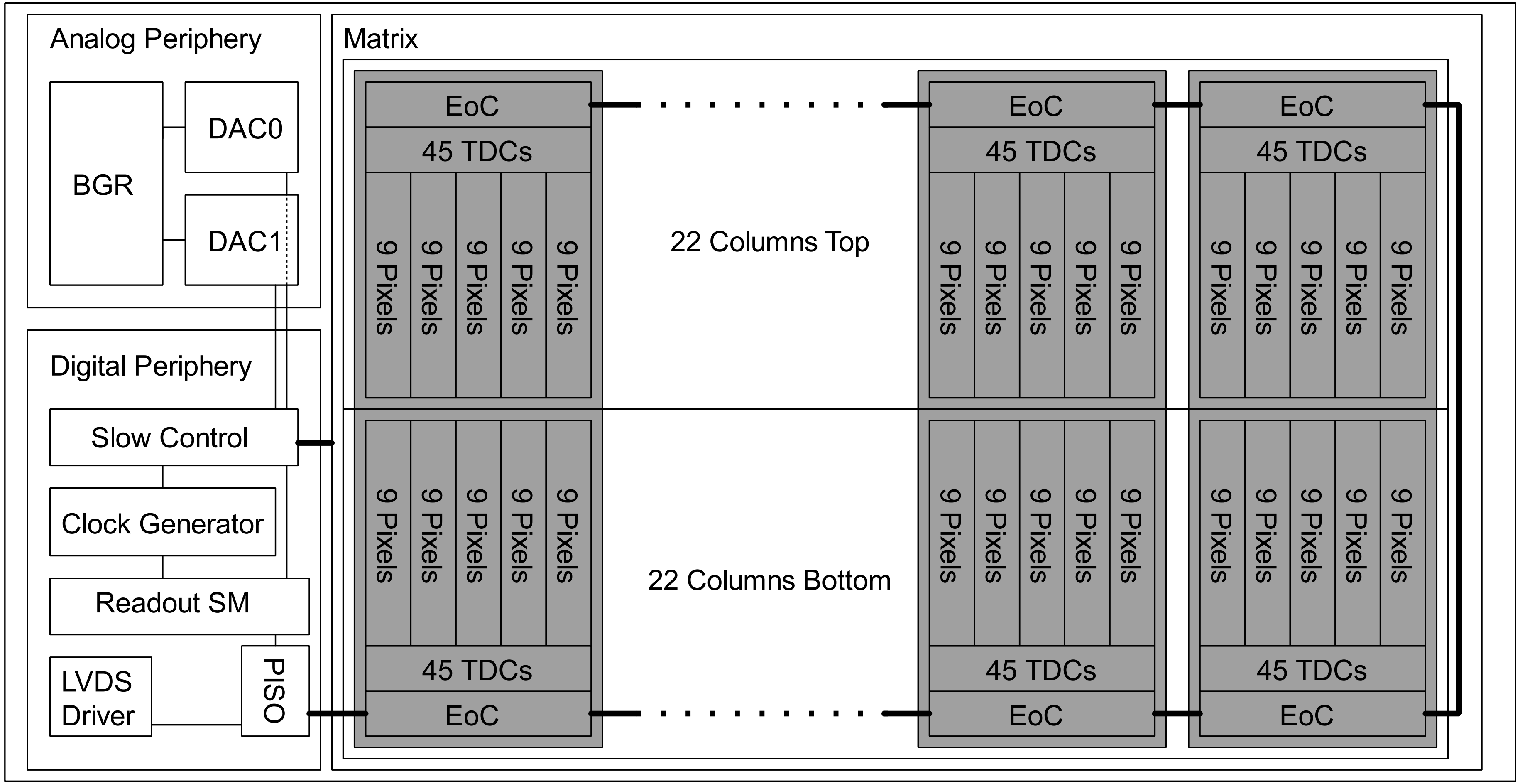
Thanks to Fabricio Alcalde and José Lipovetzky from CAB for supporting us in the design



Analog (a) vs. Digital (b) SiPM

T. Frach, G. Prescher, C. Degenhardt, R. de Gruyter, A. Schmitz, and R. Ballizany, "The digital silicon photomultiplier — Principle of operation and intrinsic detector performance," in *2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, Oct. 2009, pp. 1959–1965. doi: 10.1109/NSSMIC.2009.5402143.

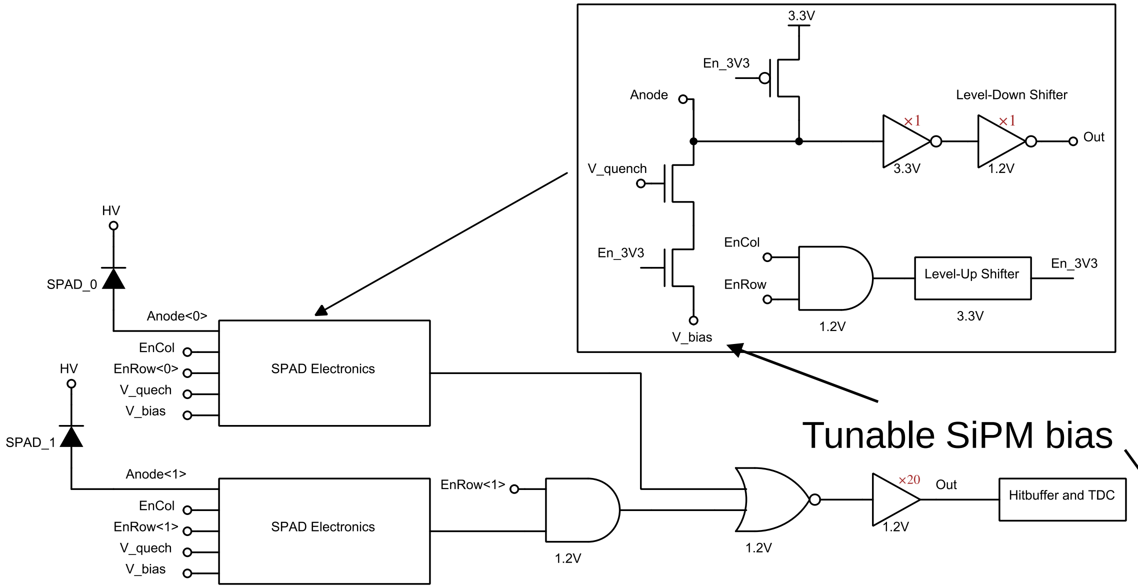
ANDESPix - a Digital SiPM for Muon Detectors



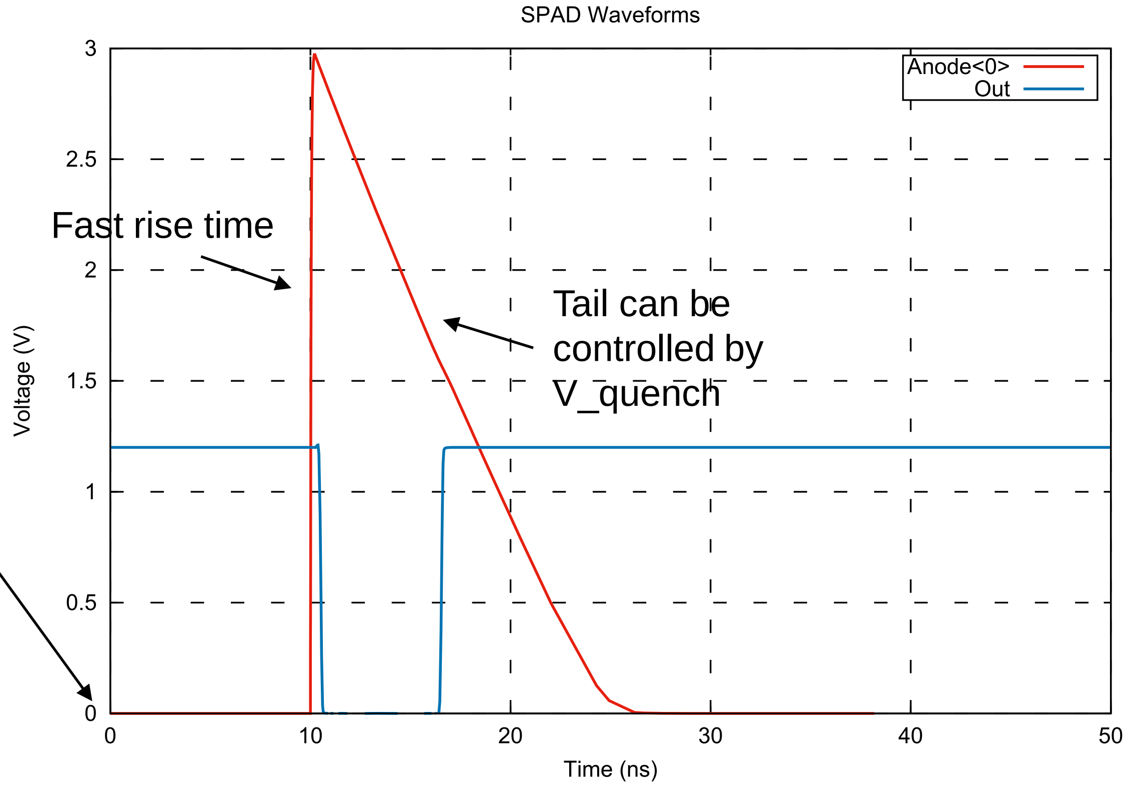
Overview of Top-Level of ANDESPix

- One time-to-digital converter (TDC) per microcell
- Technology: LFoundry 110 nm incl. SPAD addon by FBK
- Goal: 100 ps time resolution and high photon-detection efficiency (PDE)
- Pixel matrix can host two scintillating fibers, each producing <50 photons/muon

Pixel and its Electronics



Pixel of ANDESPix

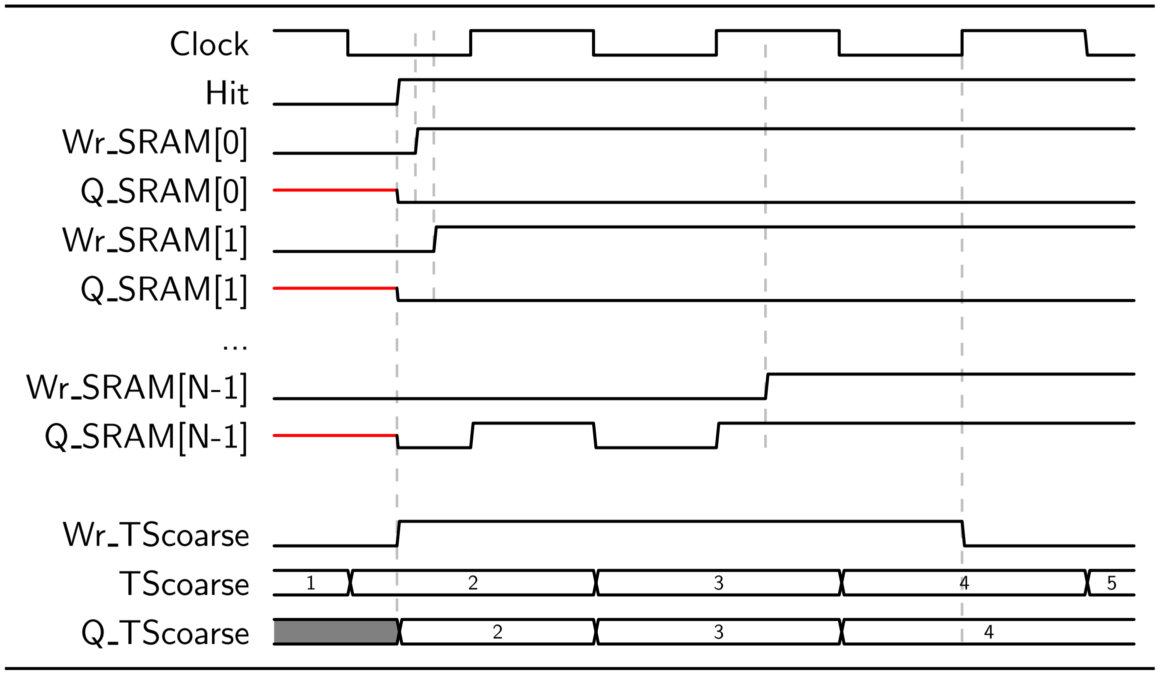


Waveform when one photon hits SPAD_0

Time-to-Digital Converter (TDC)

- 8 Transistor SRAM Cell based TDC
- TDC is split in 2 stages:
  - Coarse TDC by global gray-code timestamp counter
  - Fine TDC by delay line
    - Clock is sampled by equally distanced (<100ps) timepoints in phase to hit

    → Time between hit and clock edge can be detected
  - In case clock duty cycle is constant, TDC also works with half clock-cycle



Timing Diagram of TDC

Pixel Data and Digital Readout

- Zero-suppressed priority logic readout with hitbuffers and end of column (EoC) buffers
- Different readout modes possible
  - Asynchronous mode: read all hits all the time
  - Synchronous mode: read a certain amount of hits in a certain time frame, discard remaining
  - Self-triggered mode: only read data if internal threshold number of columns with hits is passed

Name	Size (Bit)	Description
AddrCol	7	Column Address
AddrRow	6	Row Address
ToAc	16	Time of Arrival Coarse
ToAf	20	Time of Arrival Fine
Cnt	3	Hit Counter Value
ToT	6	Time over Threshold

Data per Pixel (58 bit)

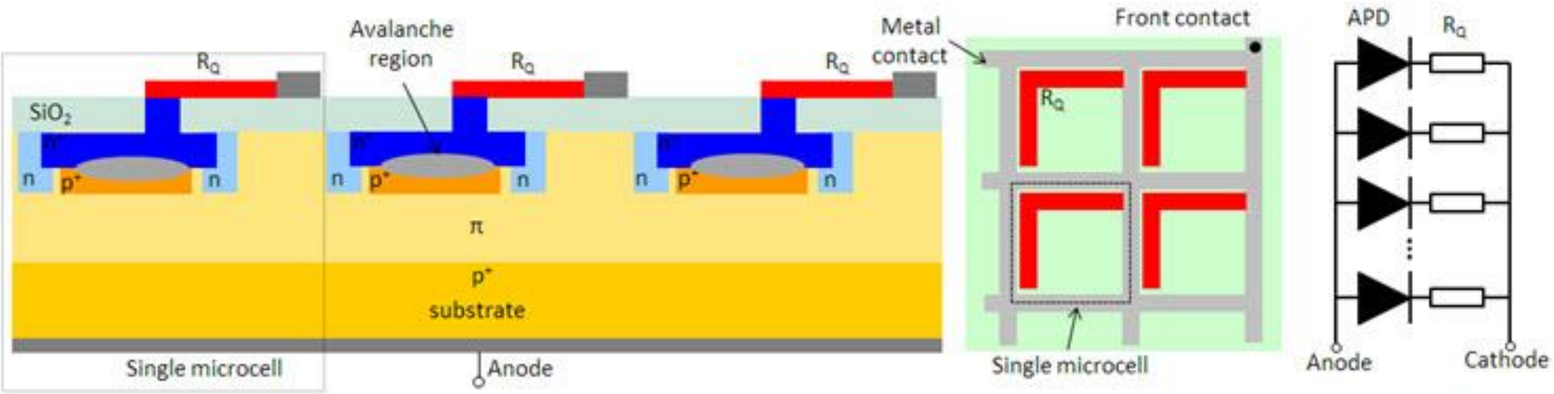
Conclusion and Outlook

- ANDESPix Taped in at LFoundry on November 6, 2023
- Production will take roughly 6 months
- Carrier Printed Circuit Board (PCB) for test will be designed
- Integration of ANDESPix on PCB
  - Bonding
  - Coating Layer
- Test of General Functionality, PDE and Timing
- Test with Muon Telescope at ITeDA

Backup

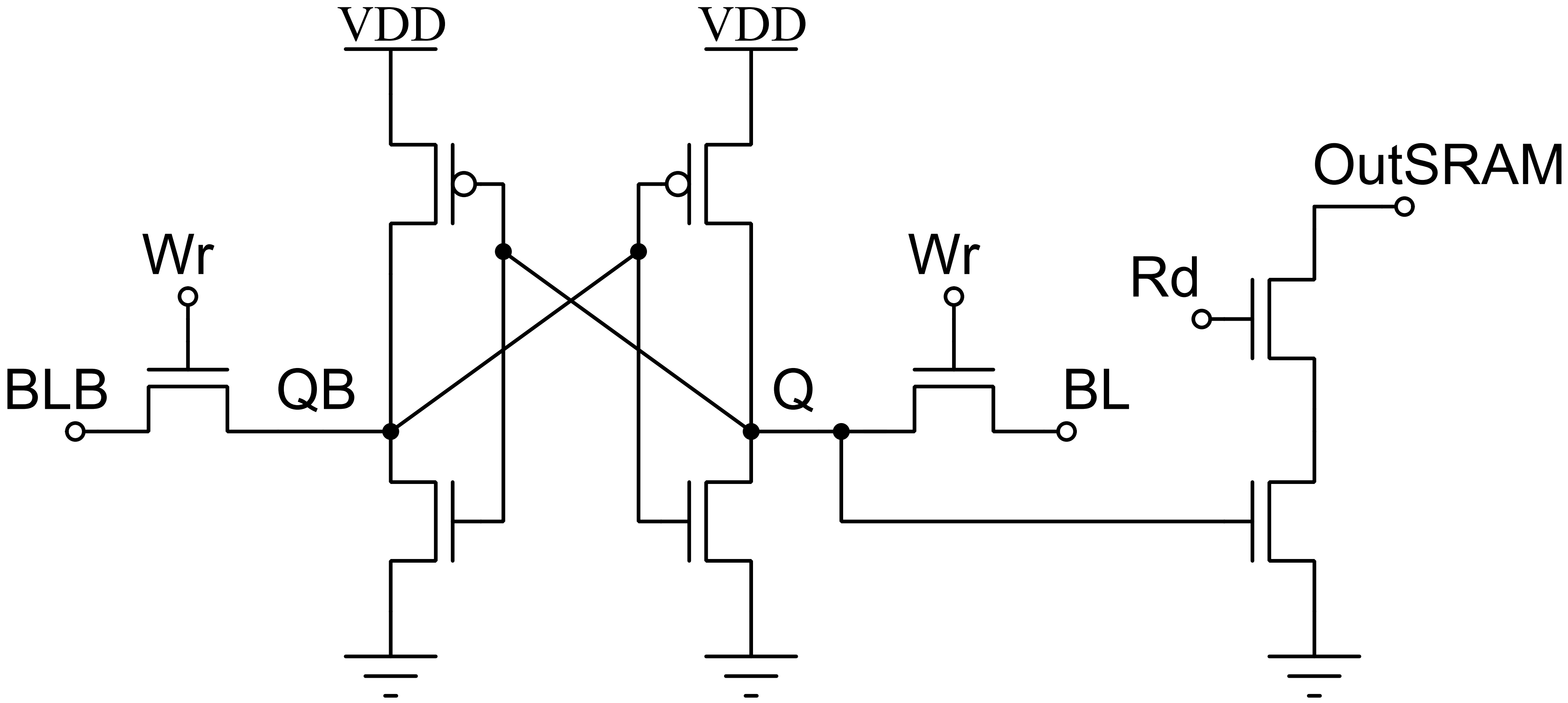
What is a SiPM?

- Analog SiPM: Array of microcells connected in parallel
- Each microcell contains a Single Photon Avalanche Diode (SPAD) connected to a quenching resistor
- SPAD is working in Geiger mode
  - When hit by a photon it generates a large avalanche current (it “fires”)
  - Avalanche current must be quenched to restore pre-hit conditions
- Output signal amplitude depends on how many SPADs fire

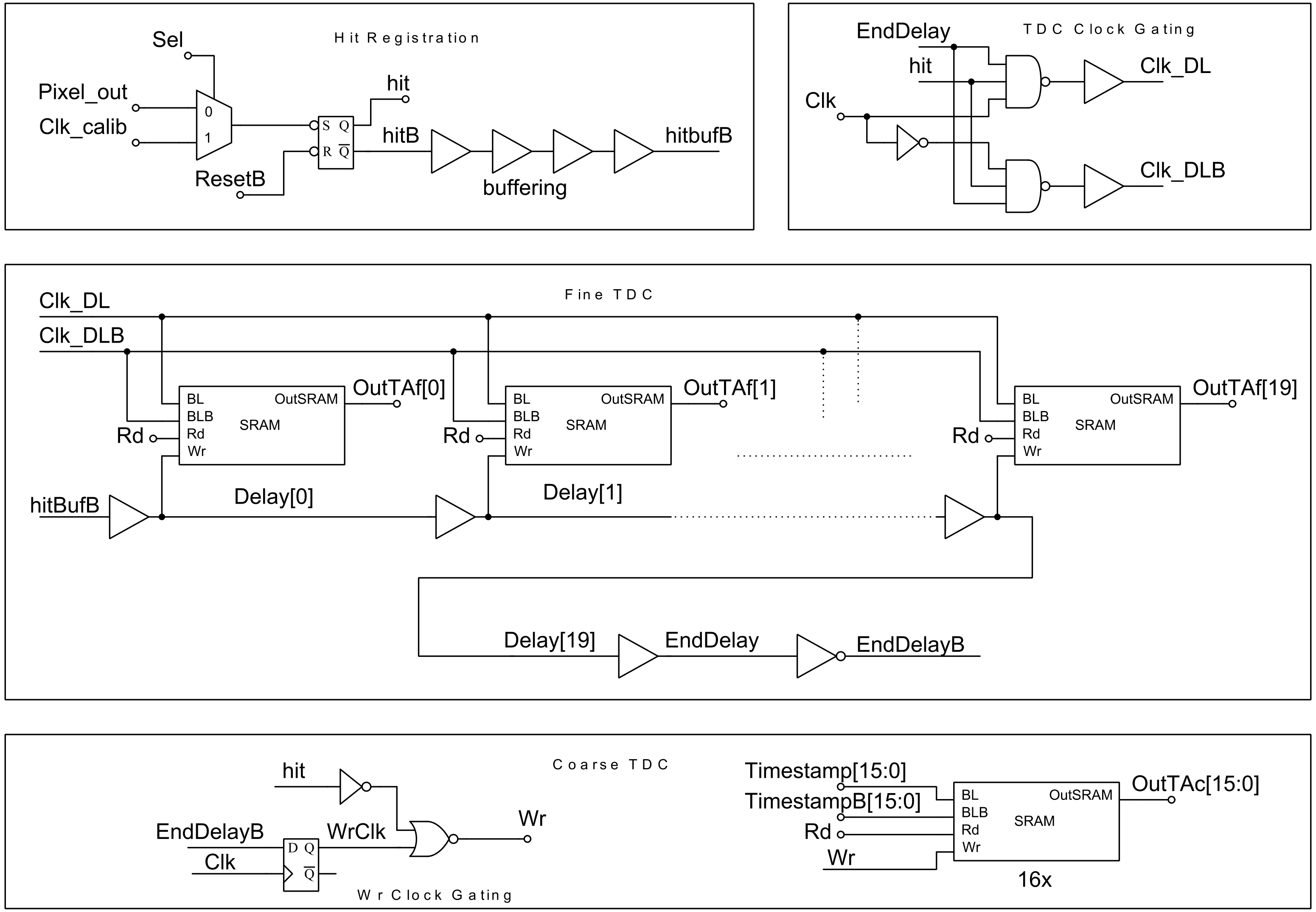


“What is an SiPM and how does it work? | Hamamatsu Photonics.” https://hub.hamamatsu.com/us/en/technical-notes/mppc-sipms/what-is-an-SiPM-and-how-does-it-work.html (accessed Nov. 04, 2022).

8T SRAM Cell



TDC


Hit Registration
Sel
Pixel_out
Clk_calib
0
1
S Q
R Q
hit
hitB
ResetB
buffering
hitbufB
TDC Clock Gating
EndDelay
hit
Clk
Clk_DL
Clk_DLB
Fine TDC
Clk_DL
Clk_DLB
BL
BLB
Rd
Wr
OutSRAM
SRAM
OutTAf[0]
OutTAf[1]
OutTAf[19]
Rd
hitBufB
Delay[0]
Delay[1]
Delay[19]
EndDelay
EndDelayB
Coarse TDC
hit
EndDelayB
Clk
D Q
Q
WrClk
Wr
Wr Clock Gating
Timestamp[15:0]
TimestampB[15:0]
Rd
Wr
OutTAc[15:0]
16x