Meeting ANDES ASIC-SiPM 20.09.2022

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Content

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- Status of SiPM
- Detector System
- ASIC
- Schedule for ASIC Submissions

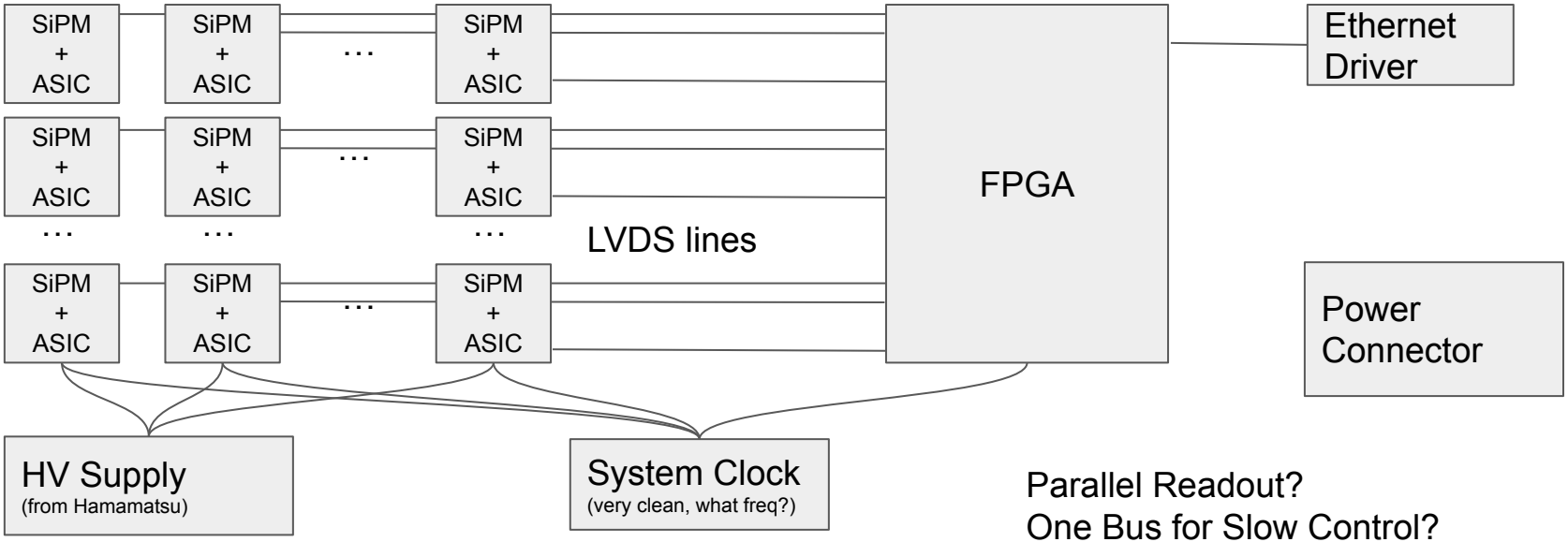
Organization

- It is difficult to find all presentations on the Indico because one has to go through all meetings
- All documentation can be accessed on on the Design Server (ipeasic1.ipe.kit.edu)
  - /home/public/shared_cadence_designs/IHP/ANDES_SiPM_ASIC/doc/
- I will write a documentation/manual of the ASIC in overleaf
  - https://www.overleaf.com/read/xnxqwdncfrrn

SiPM

- What is the status of contact with FBK?
- DESY is doing a very similar project main difference that we have a TDC for each pixel
  - https://fe.desy.de/fec/projects/high_energy_physics/digital_sipm_pixel_detector/
  - And a talk a the MT-Meeting: https://indico.desy.de/event/33132/contributions/128252/
  - Maybe we can exchange with those people and talk about their experiences
  - Maybe if FBK is not able to deliver in time we can try to get in contact with MPG-HLL

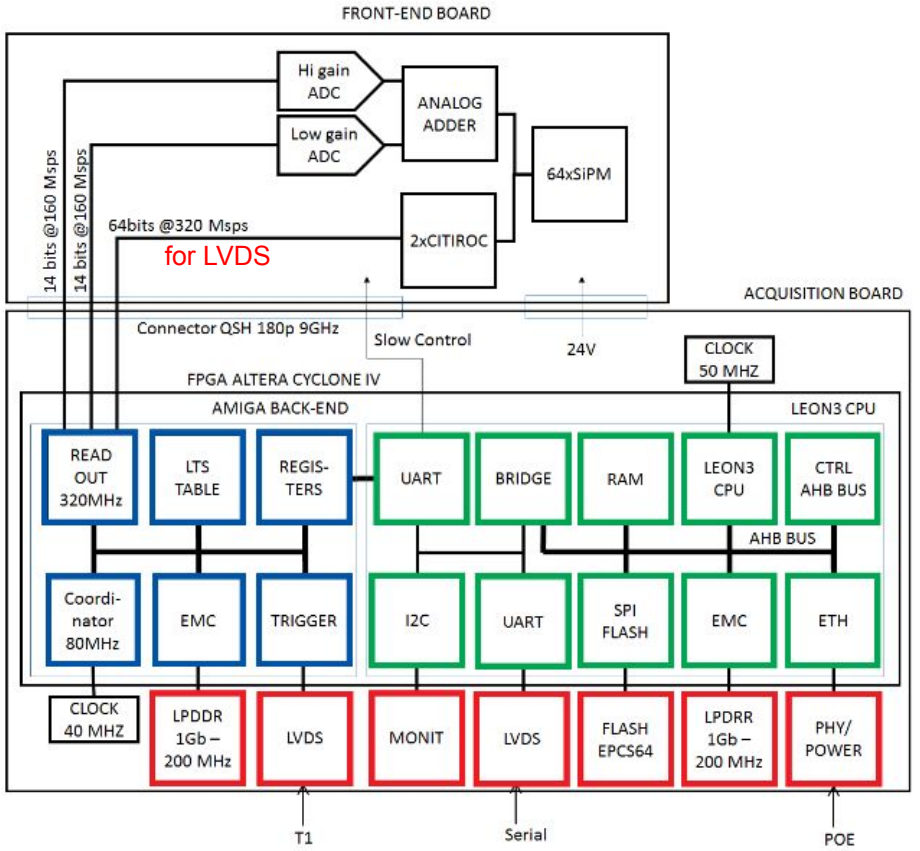
Detector System (Basic Needs)



Parallel Readout?
One Bus for Slow Control?
How to address each chip?
Shift Register with all chips?

Should we use the AMIGA DAQ Board?

- Is the ALTERA CYCLONE IV still available?
- System Clock available for front end?
- Any other small FPGA/Microcontroller Board should be enough, too
  - Task of it would be only to do the slow control and receive LVDS signals and store/transfer them

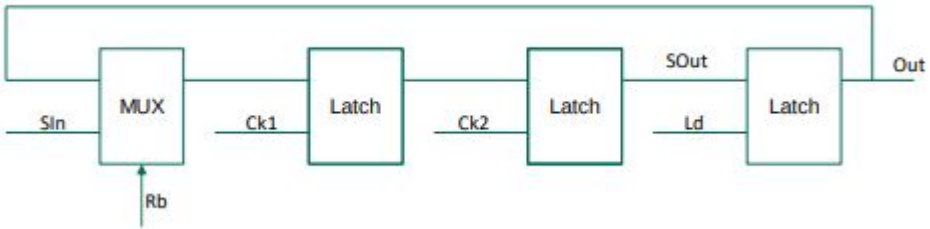


Detector System - remarks

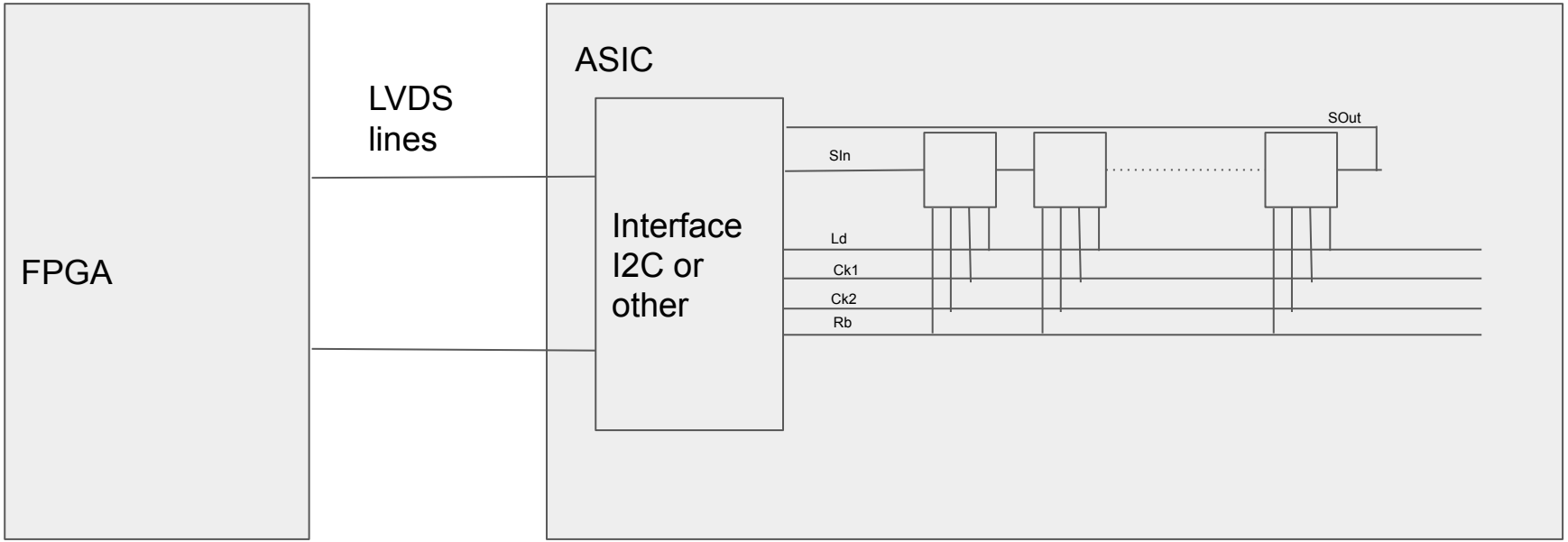
- ASIC will be wirebonded and then put into optical cement
  - Hamamatsu SiPM is connected in the same way
- Complete Setup has to be put into a dark box
- Complete system as small as possible to have high fill factor of the complete detector in ANDES

ASIC - Slow Control

- 1 or 2 line interface from FPGA to shift register on chip (I2C or different)
  - shift register is working on PicoPix1 and is custom made
  - shift register cells can be placed everywhere and they will be connected to analog power supply to avoid injecting noise
  - If necessary we can use similar approaches than Ivan to reduce size of in pixel memory
    - https://adl.ipe.kit.edu/english/26.php
  - shift register needs read back capabilities to regularly check if configuration is still valid
  - connect several ASICs in series to avoid address issues???



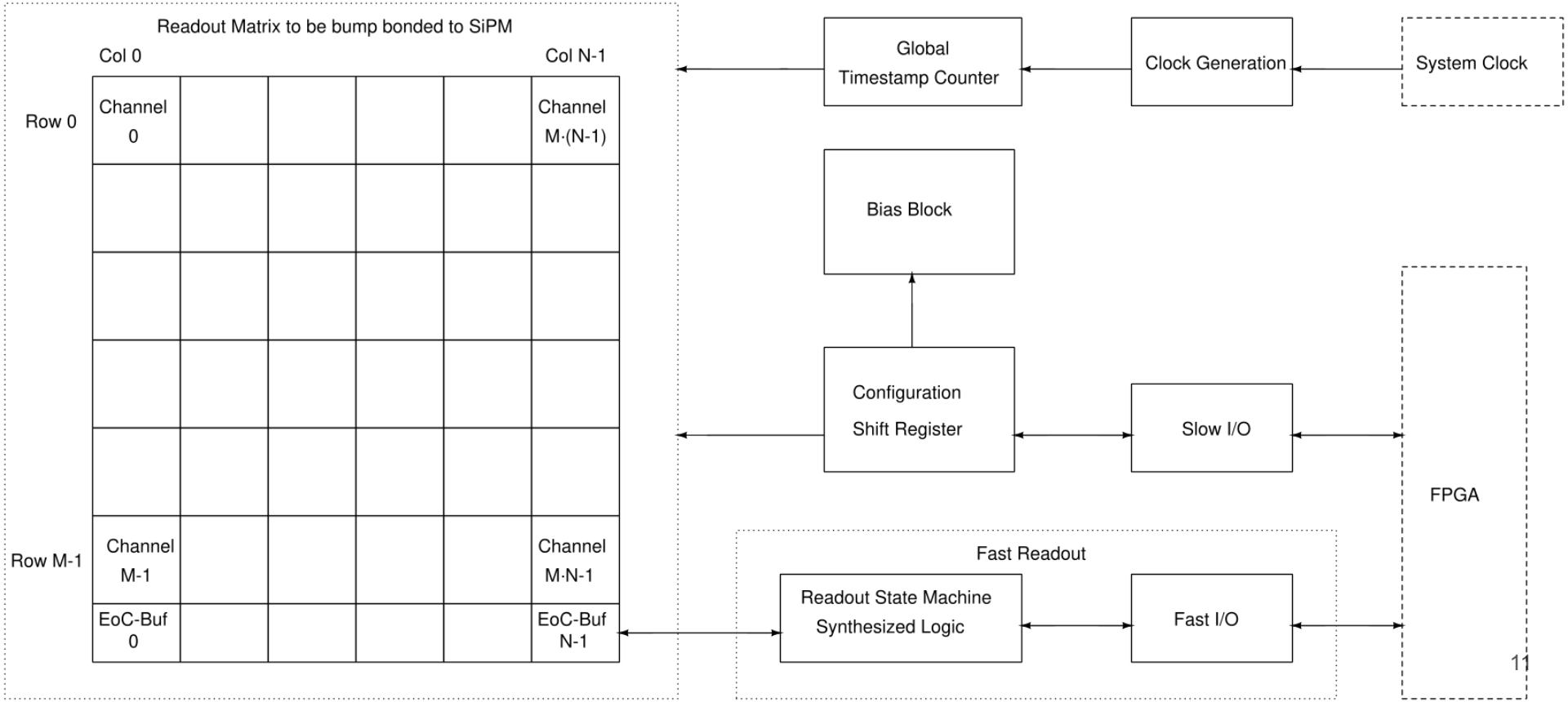
ASIC - Slow Control



ASIC - Zero Suppression and Readout

- It consists of a hitbuffer in pixel to control the TDC, a (end of) column buffer for parallelization and a readout state machine at the periphery
- hitbuffer needs to create a hit flag and an OR of those flags for one column
- in statemachine:
  - AER logic to reduce amount of data to transmit
  - fixed order of bits in PISO: Address, ToA, ToT, Channel Counter (3 bit) so we can cut the later ones
- In channel hit counter (3 bit) could be useful to detect pile up in case there is space remaining inside the channel
- readout speed as slow as possible to reduce power!
  - maybe programmable?

ASIC top overview



ASIC - Work distribution

- Alexander + Fabricio: analog and full custom digital part
- Alan + Manuel + Michele + new student: synthesized digital part at periphery and FPGA
  - I can describe you how I did the readout of the PicoPix1 as a starting point
- Alexander: Chip Top

Is this okay?

Schedule for ASIC Submissons

First submission of new TDC and Comparator together Ivan???

25 Nov for Europractice Registration

Submission of first demonstrator

Turn Back Dates

TAPE IN	SGB25	SG25		SG13					
	V / RH**	H3	EPIC	S (C)	MEMRES	SCu	G2Cu	G2	G3Cu
Nov 7, 22	***	***	Jun 19						
Dec 12, 22				May 16*	May 30	May 19*	May 12	May 23*	
Feb 20, 23						Jul 6	Jul 21		Jul 30
Apr 3, 23	Jul 17*	Jul 12	Nov 16						
Jul 3, 23				Oct 26*	Nov 9	(Nov 28)	(Dec 4)	Nov 10	
Aug 7, 23	(Nov 15)	(Nov 20)*							
Sep 18, 23				Feb 1		Feb 1	Feb 16	Mar 5*	
Nov 6, 23			Jun 17						
Dec 11, 23				May 14*	May 28	May 23*	May 23	May 7	Jun 6

* Runs with lower priority

** TAPE IN for digital blocks is 1 month before standard TAPE IN

*** TAPE IN available on special request

Source: https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/schedule-price-list