Karlsruher Institut für Technologie

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Backend Design of the Read-Out System for Cryogenic Particle Sensors

DDAp/DDEIT and HIRSAP Workshop 2022 – UNSAM

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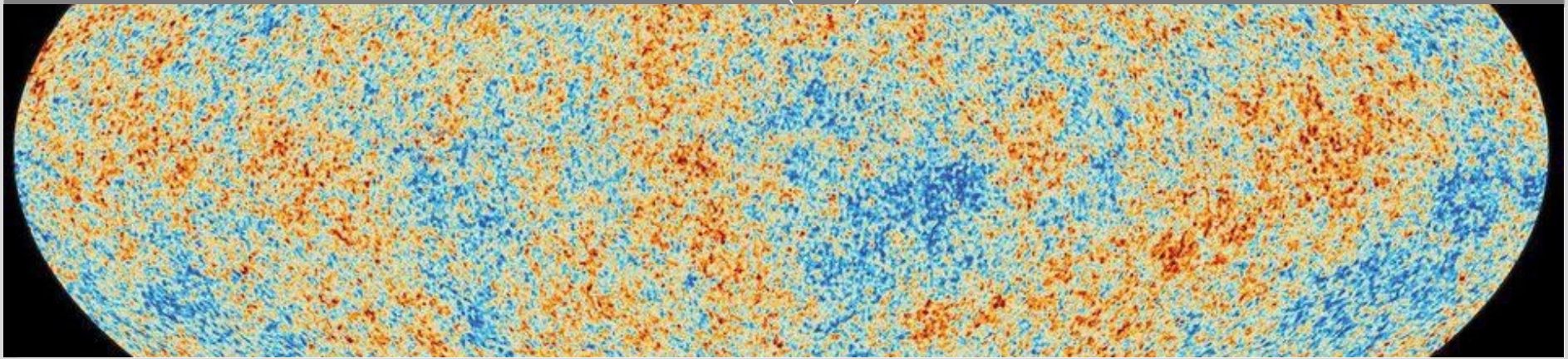
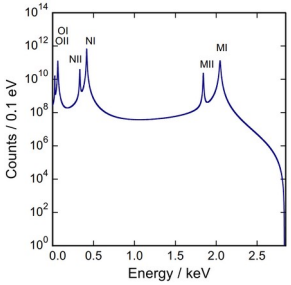
INSTITUTO EN TECNOLOGÍAS DE DETECCIÓN Y ASTROPARTÍCULAS (ITeDA)

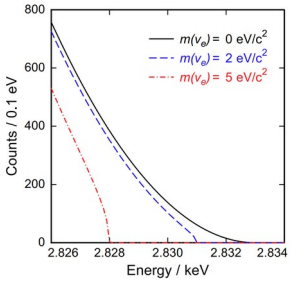


Thesis goals

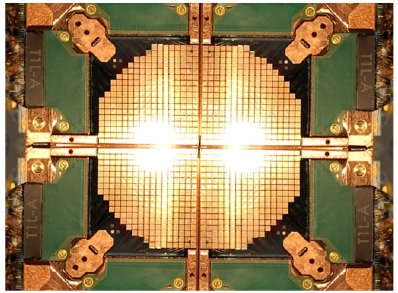
Contribute to the development of a read-out system for cryogenic sensors, multiplexed in the frequency domain (FDM) and which allows:

1) **Real Time processing, of several sensors (>= 1000),**
2) **Scalable: minimizing the used resources (FPGA specific).**



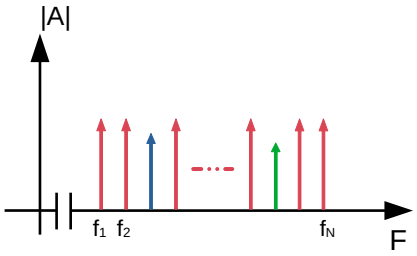


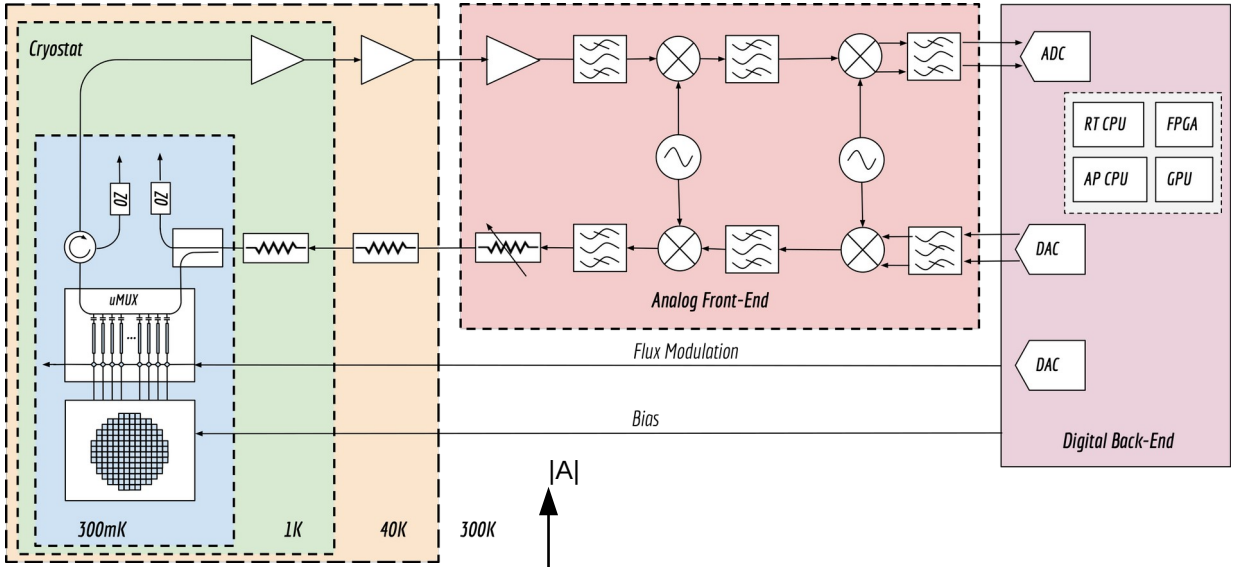
QUBIC Telescope in the Integration Lab. in Salta, Argentina. Performing the atmosphere profiling before starting the Moon scan during August.

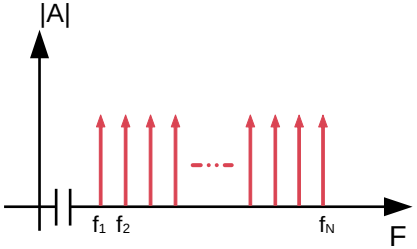


QUBICs focal plane

Read-Out Electronics







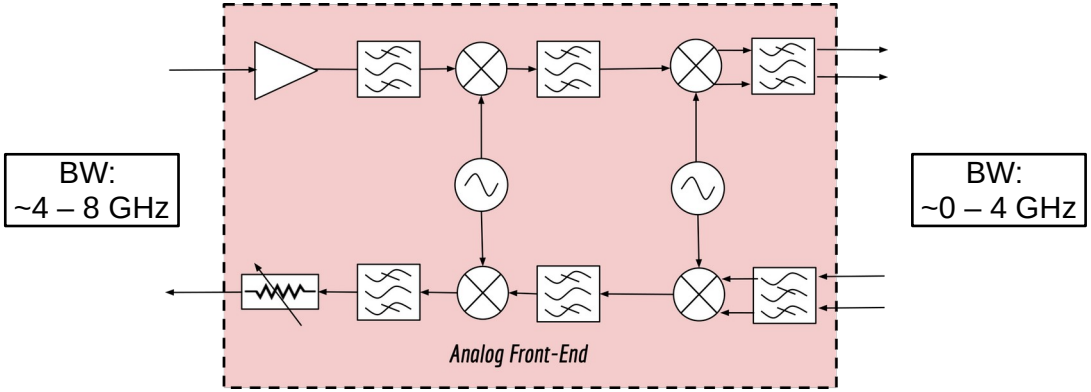
QUBIC requirements:

- Nº of Ch. (sensors): 1024 (per focal plane),
- Channel spacing: 4 MHz,
- Signal bandwidth: < 200 kHz.

ECHo requirements:

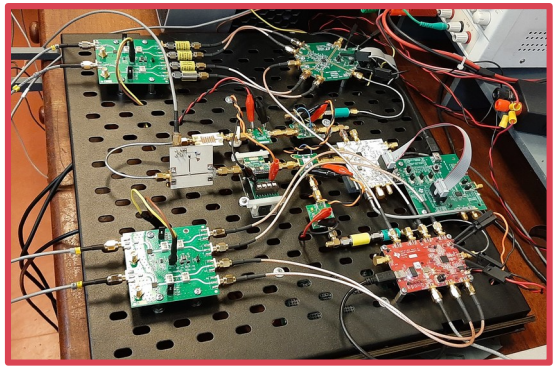
- Nº of Ch.: 6000,
- Channel spacing: 10 MHz,
- Signal bandwidth: ~1.6 MHz

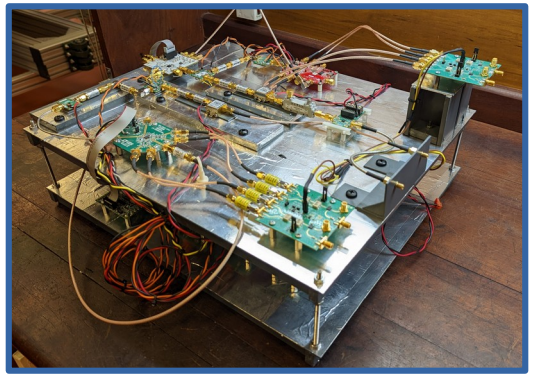
Radio Frequency Front-End (RF-FE)



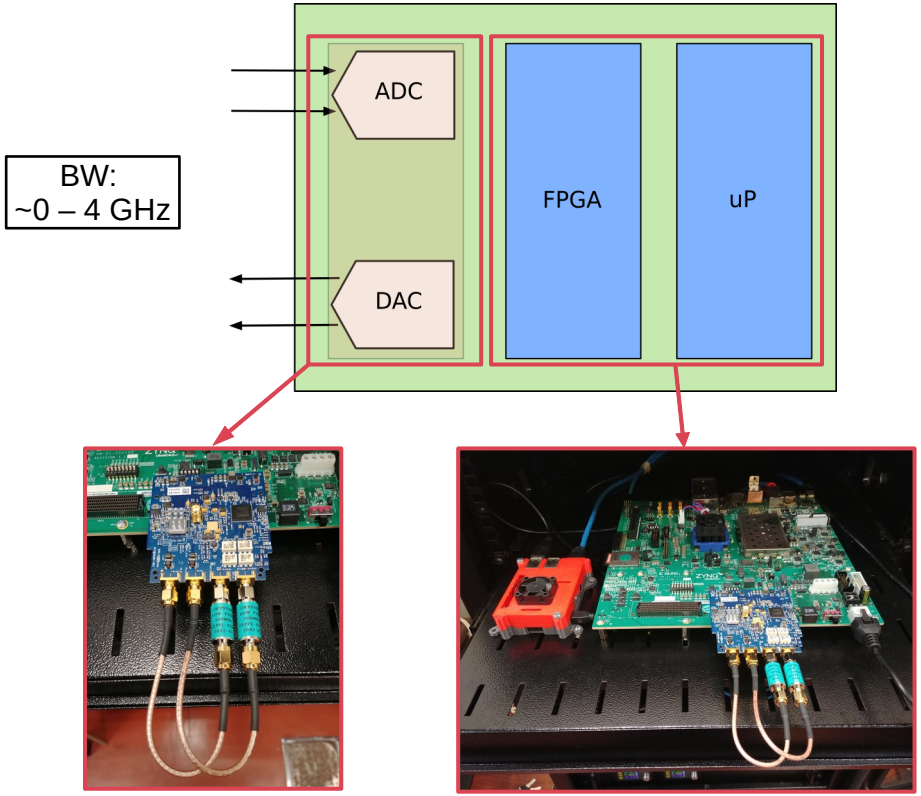
Main goal:

- Up-conversion,
- Down-conversion,
- Preserve a high SNR,
- Merge/split the spectrum





Digital Electronics Back-End (DE-BE)

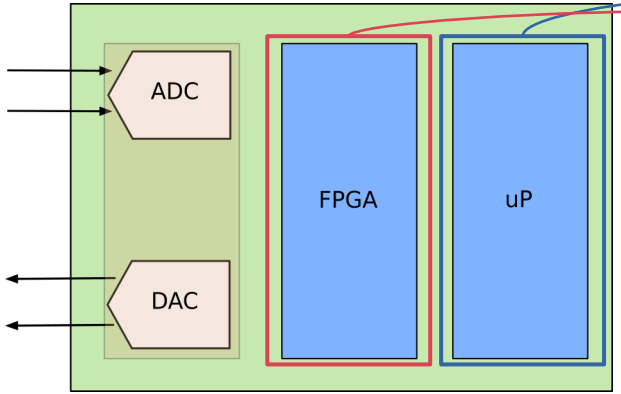


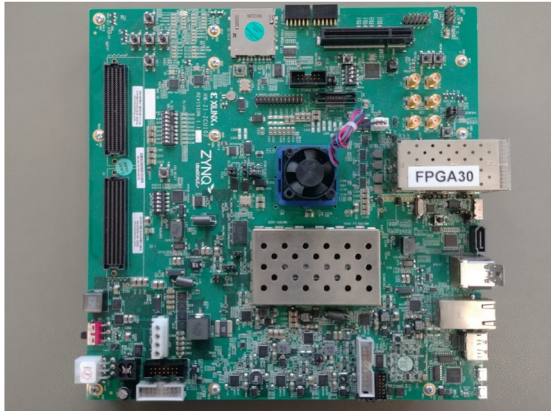
Main goal:

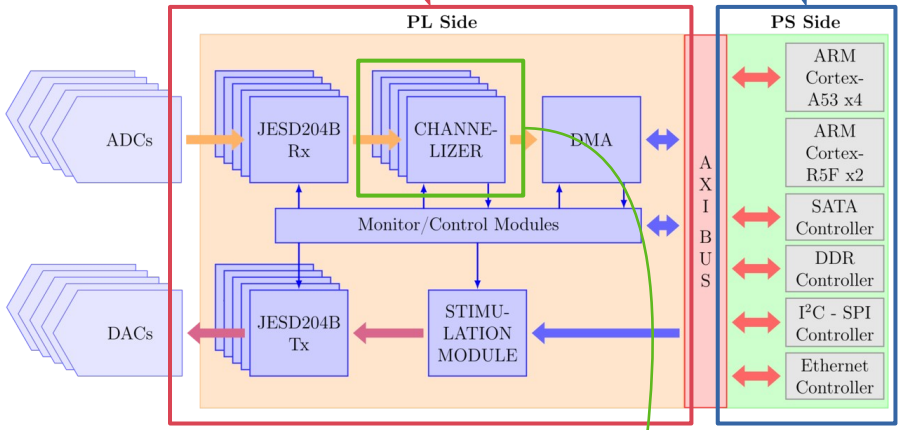
- Generate base-band (BB) multitonal signals,
- Read them back after the RF-FE,
- Pre-process of the samples,

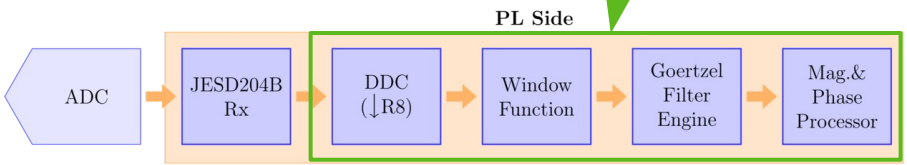
- Converters board: AD-DAQ2FMC (from Analog Devices):
  - ADC: AD9680 @ 1 GSPS (14 bits)
  - DAC: AD9144 @ 2.8 GSPS (16 bits)
- Xilinx ZCU102:
  - Zynq UltraScale+ MPSoC (9eg)

Digital Electronics Back-End (DE-BE)



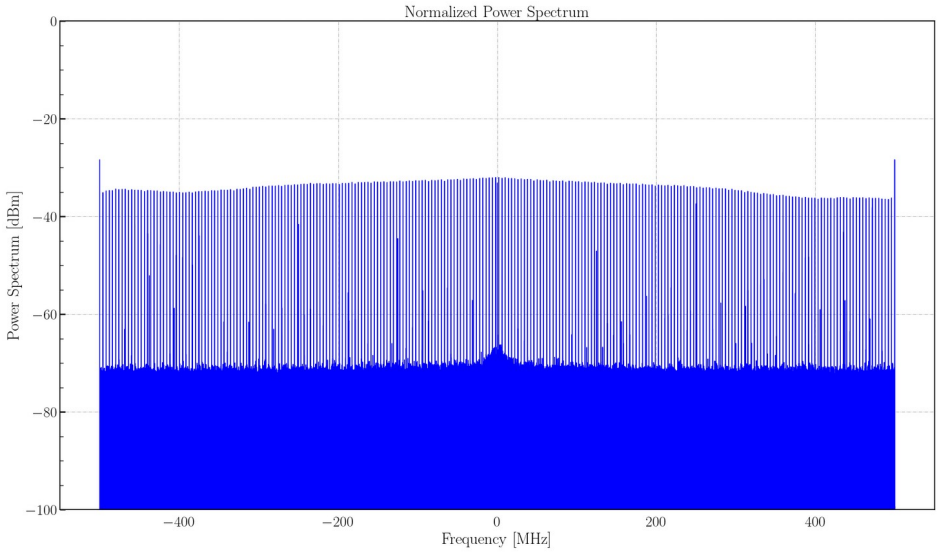


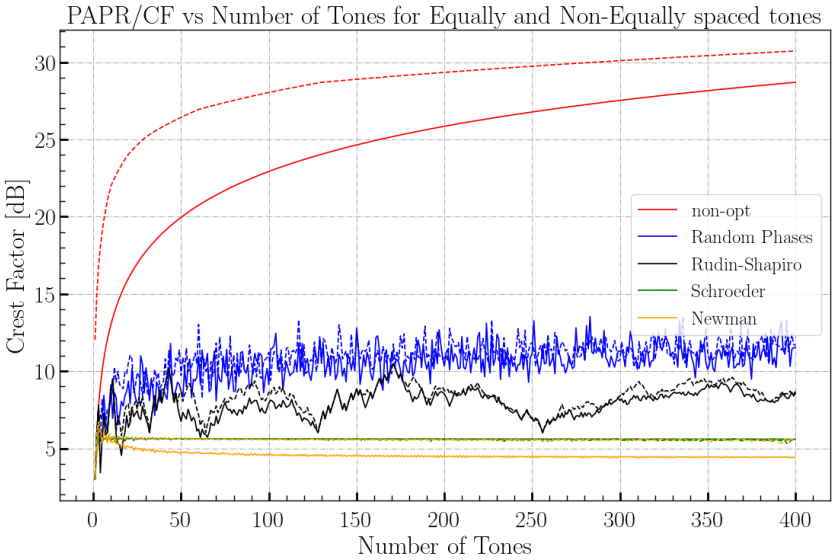




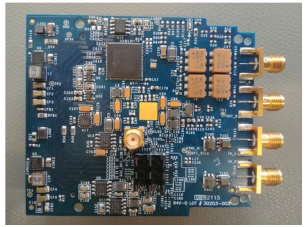
Status of the experiments: preliminary results

Signal Generation with low PAPR/CF

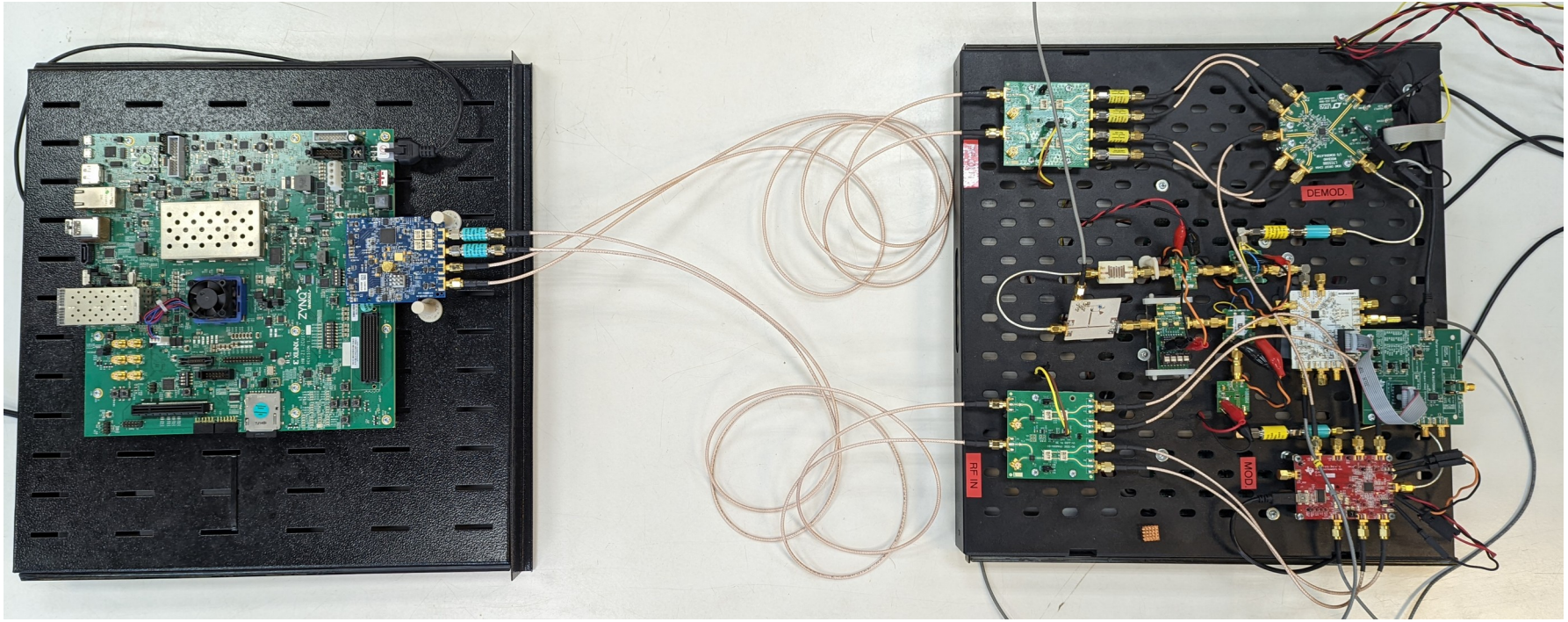




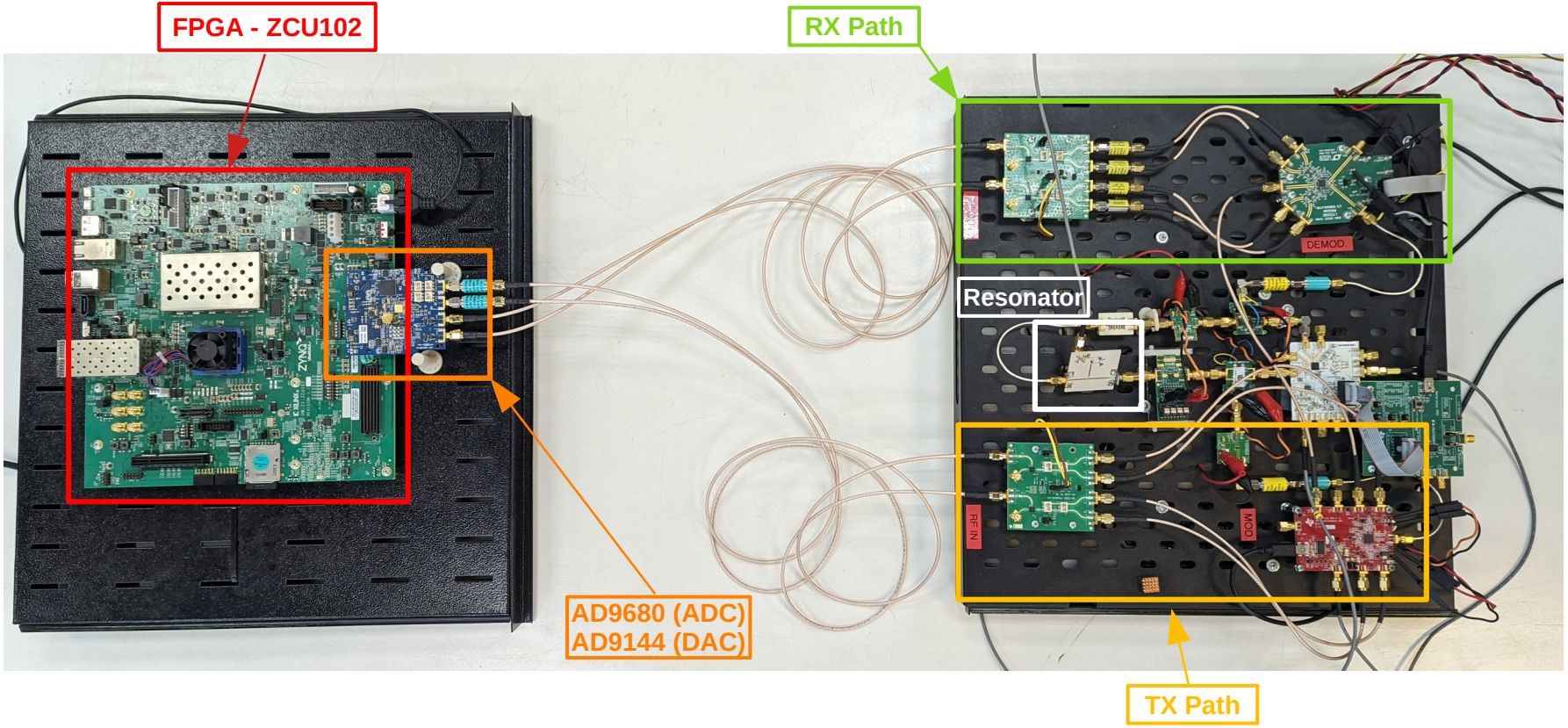
- Generation of multitonal signal with low PAPR/CF (CF ~ 1.98),
- Other algorithms for achieving low PAPR and performing IQ correction/balancing, are being studied,
- The DAC Roll-Off and Low Pass Filters response, can be appreciated in the left plot.



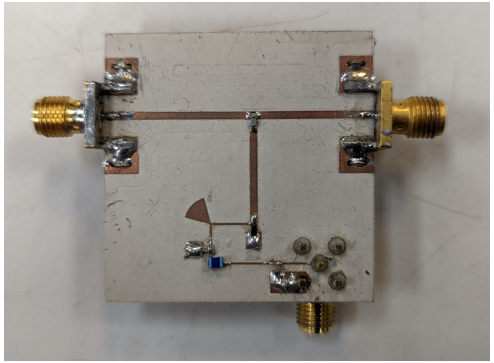
Experimental Setup: DB + RF + Res.

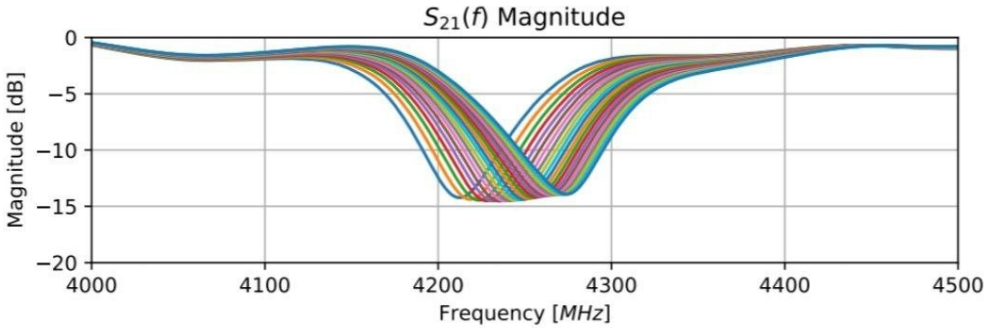


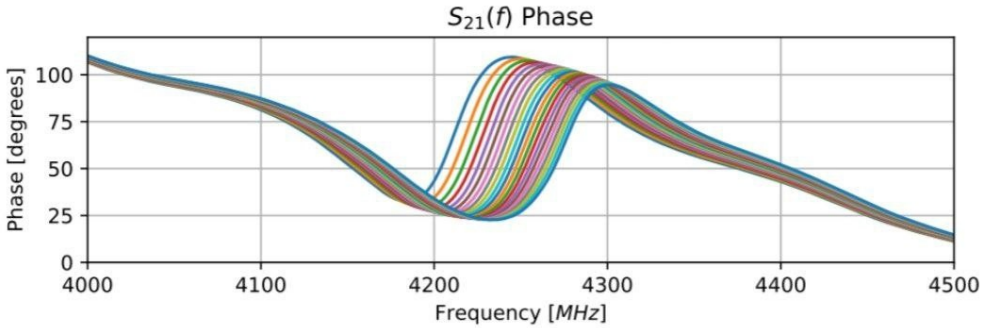
Experimental Setup: DB + RF + Res.



Experimental Setup: DB + RF + Res.



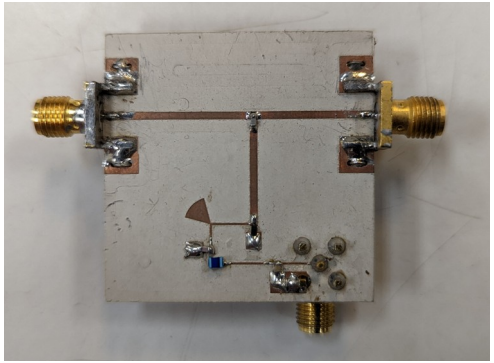


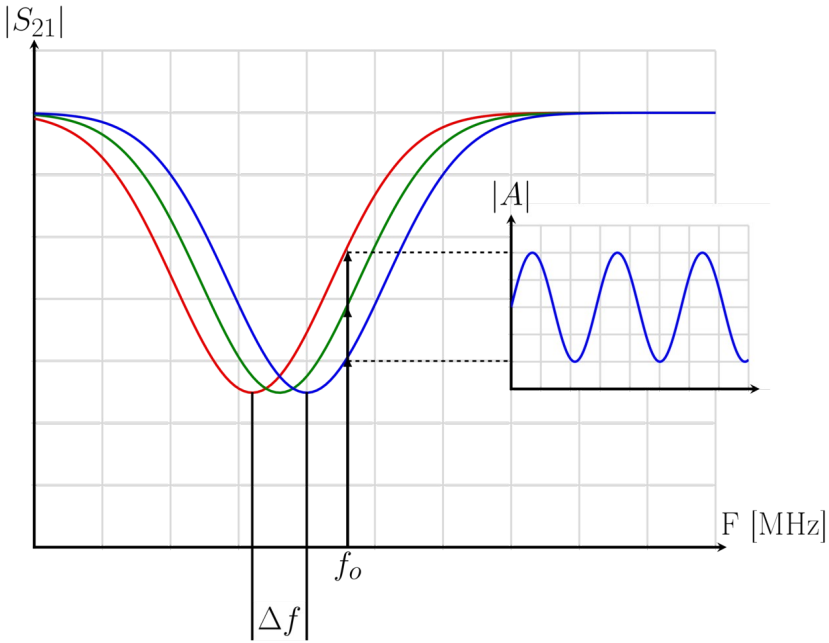


- Built resonator for read-out electronics characterization. It‘s based in a varicap, which is controlled by voltage from 0 to 10 Vdc.
- Operates between (approx.) 4210 – 4275 MHz

This plot is a Manuel García Redondo’s courtesy

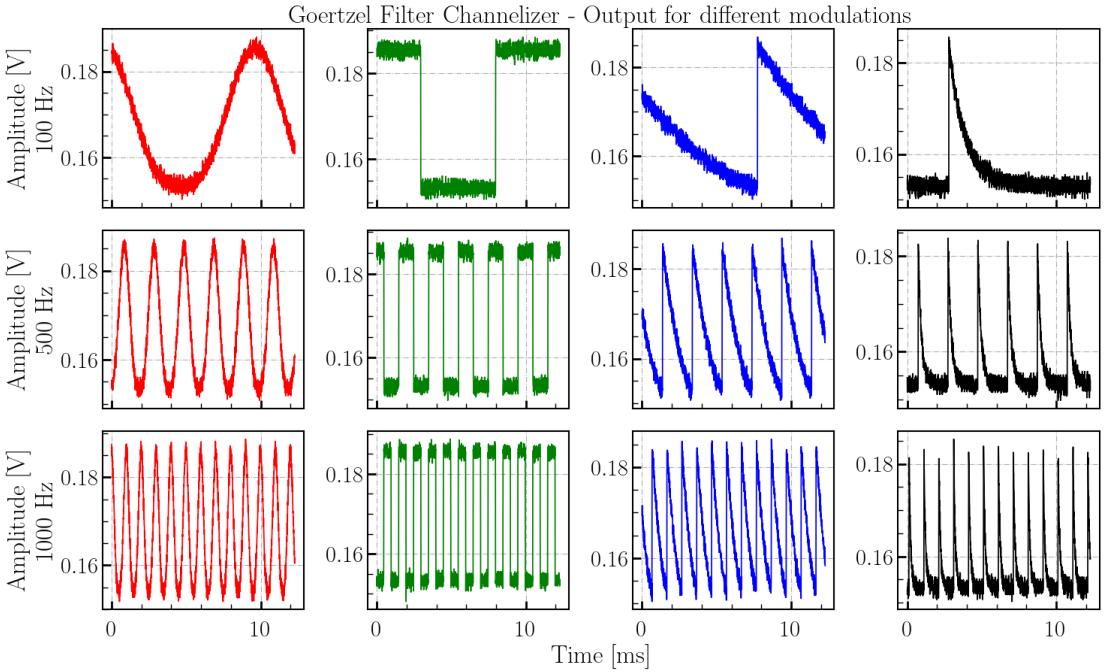
Experimental Setup: DB + RF + Res.





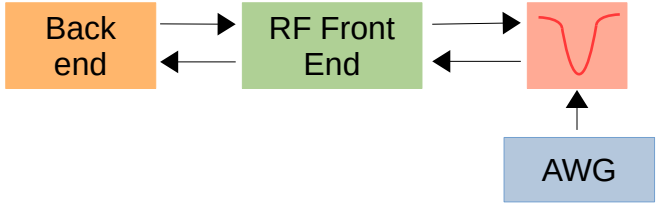
Modify the resonance frequency with an external source, varying the control voltage signal with different signal types.

Signal Processing – Resonator readout with Flux-Ramp Modulation (FRM) approach

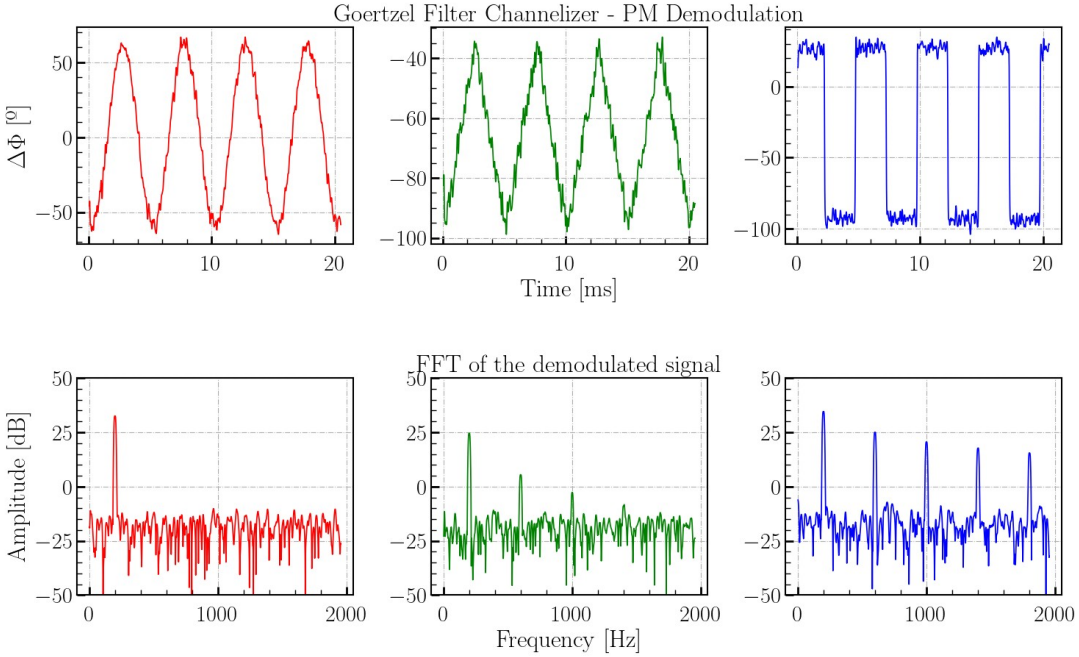


Experiment:

- Tested: sinusoidal signal, rectangular, ramp and an exponential, at different frequencies (from 100 Hz to 50 kHz),
- Successfully demodulated the resonators response in all cases.



Signal Processing – Resonator readout with Flux-Ramp Modulation (FRM) approach + detector emulation (extra PM)



Experiment:

- Tested: **first modulation** is a **30 kHz** sinusoidal signal attacking the resonator, and that modulation signal has a **PM of 60 degrees at 200 Hz** with different signal types: sinusoidal, triangular and square,
  The 60º (120º from top to bottom) can be appreciated in the figures.
- Successfully demodulated detector signal from the resonators response in all cases.

Resources consumption

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Resource consumption of channelizer modules

Direct Down Converter			
Component	DSP	LUTs	BRAM / LUT
Complex multiplier	3	92	- / -
CIC Decimation filter	-	999	- / -
FIR Compensation Filter	16	160	- / 398
Local Oscillator	-	118	2 / 2
Total	**19**	**1373**	**2 / 400**

Goertzel Filter Bank			
Component	DSP	LUTs	BRAM / LUT
Iterative section	2	229	- / 94
Non-iterative section	12	322	- / 96
Total	**14**	**551**	**- / 190**

Window Function			
Component	DSP	LUTs	BRAM / LUT
Multiplication array	**2**	**60**	**4 / 1**

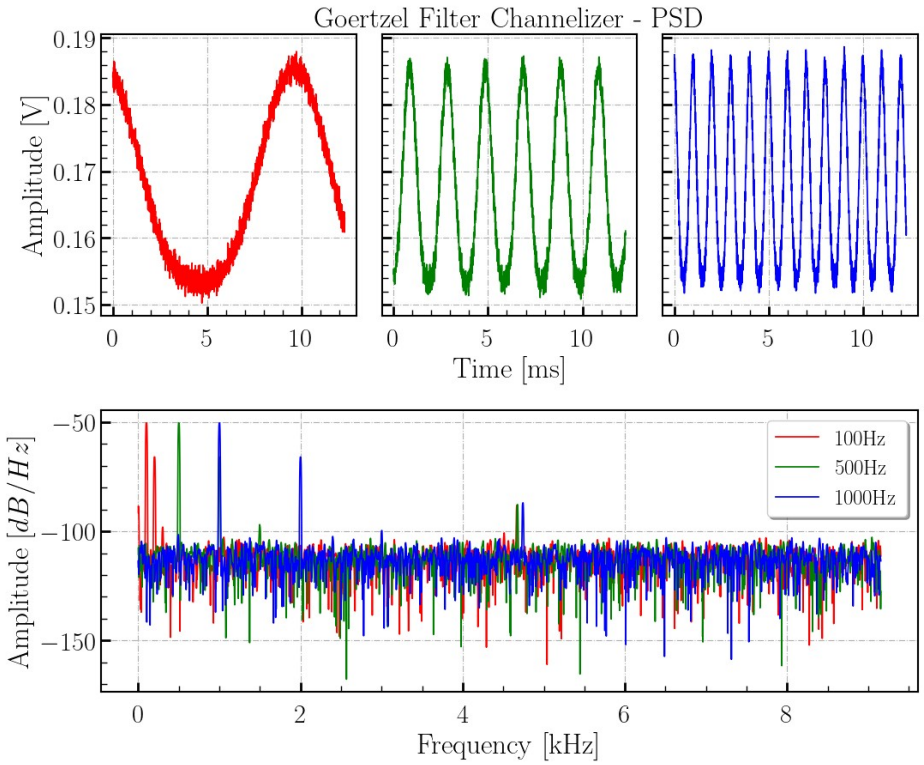
Current benchmark:

- logic@250 MHz → ~1 DSP Slice / channel (tone),
- Prototype based in **ZU9EG***, but one based in an **ZU11EG** would fulfill all requirements,
- logic@500 MHz → ~0.5 DSP Slice / channel (tone) (will be investigated as it **considerably save resources in this approach**).

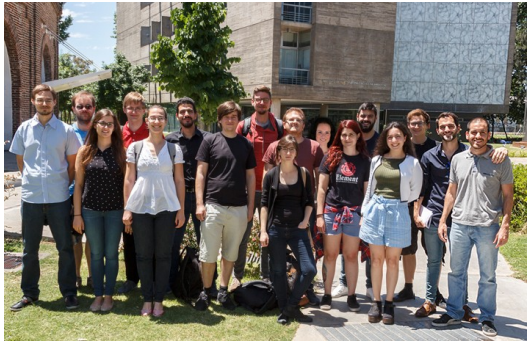
*for 4 channels: DSP Slices: ~1.4 % | Logic Cells: ~0.36 % | BRAM: ~ 1% → for 400 channels 98% of DSP Slices, 65% of BRAM and 115% of Logic Cells at 250 MHz, but the main issue is the HT ports which are insufficient for 1 DAC and 1 ADC more.

Planned measurements and work

- Channelizer noise characterization: quantization noise, ENBW, etc.
- Measurements with cryostat.



¡¡Muchas gracias!!
¡¡Vielen Dank!!



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PTB
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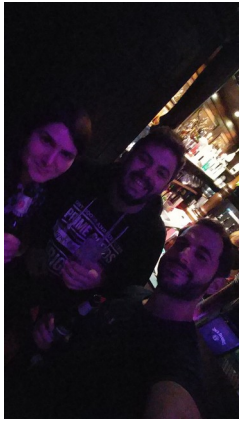
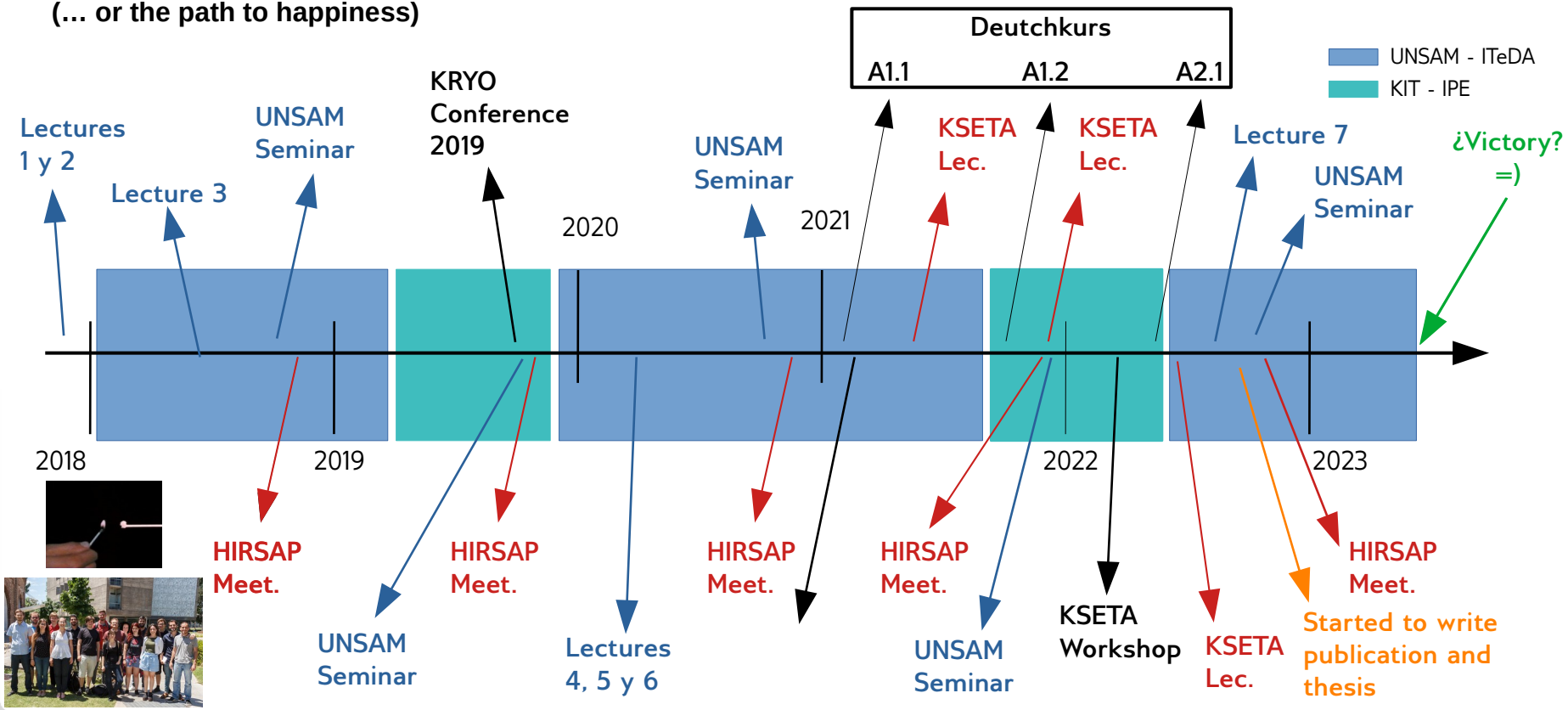
KRYO 2019
29. September – 1. Oktober 2019



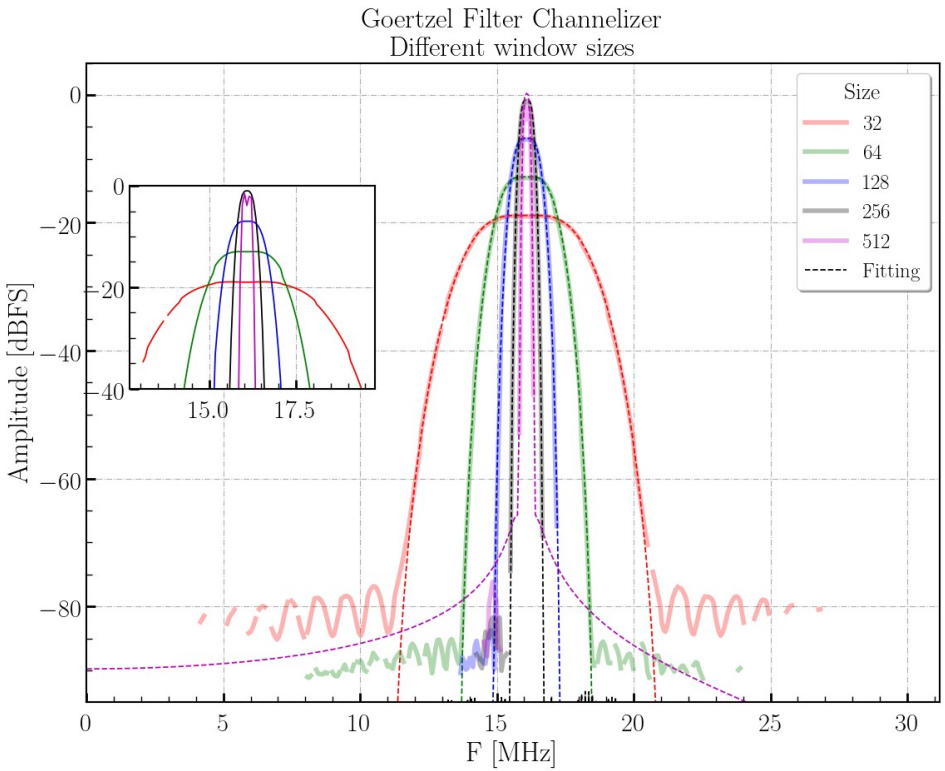
Back Up

Duties as a HIRSAP student

(… or the path to happiness)

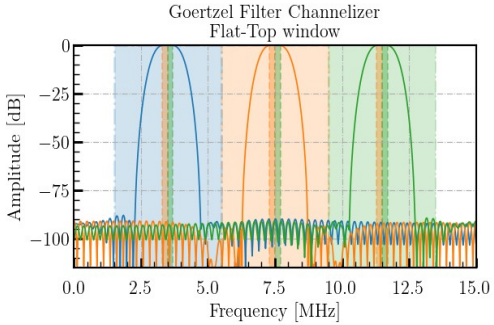


Channelizer Frequency Response



Perfomance with different window sizes:

- Implemented firmware: 4 DDCs with 1 G.F. module → 4 tones to be processed in parallel,
- Frequency sweep: 0 MHz to 31.25 MHz (step = 0.065 MHz),
- Window function:
  - Flat-Top.
- 5 different window sizes:
  - 32, 64, 128, 256, 512 samples.



Used Resources – 4 channels (full)

Name	CLB LUTs (274080)	CLB Registers (548160)	CARRY8 (34260)	F7 Muxes (137040)	F8 Muxes (68520)	CLB (34260)	LUT as Logic (274080)	LUT as Memory (144000)	Block RAM Tile (912)	DSPs (2520)
system_top	12.23%	8.29%	3.21%	0.21%	0.06%	23.11%	11.01%	2.31%	8.29%	39.36%
i_zcu102_ddr4_daq2_wrapper (zcu102_ddr4_daq2_wrapper)	12.05%	8.15%	3.19%	0.21%	0.06%	22.72%	10.85%	2.29%	8.15%	39.36%
zcu102_ddr4_daq2_i (zcu102_ddr4_daq2)	12.05%	8.15%	3.19%	0.21%	0.06%	22.72%	10.85%	2.29%	8.15%	39.36%
zynqmp (zcu102_ddr4_daq2_zynqmp_0)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
zynq_rst (zcu102_ddr4_daq2_zynq_rst_0)	<0.01%	<0.01%	0.00%	0.00%	0.00%	0.03%	<0.01%	<0.01%	<0.01%	0.00%
zynq_intr_concat (zcu102_ddr4_daq2_zynq_intr_concat_0)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
vcc_cell (zcu102_ddr4_daq2_vcc_cell_0)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
stimulation_0 (zcu102_ddr4_daq2_stimulation_0_0)	0.24%	0.13%	<0.01%	0.00%	0.00%	0.69%	0.24%	0.00%	0.13%	14.04%
spi_csn_concat (zcu102_ddr4_daq2_spi_csn_concat_0)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
sample_mapper_dac (zcu102_ddr4_daq2_sample_mapper_dac_0)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
sample_combiner_0 (zcu102_ddr4_daq2_sample_combiner_0_0)	0.02%	0.02%	0.00%	0.00%	0.00%	0.08%	0.02%	0.00%	0.02%	0.00%
pimc (zcu102_ddr4_daq2_pimc_0)	0.03%	0.03%	0.06%	0.00%	0.00%	0.17%	0.03%	0.00%	0.03%	0.00%
peripheral_interconnect (zcu102_ddr4_daq2_peripheral_interconnect_0)	0.58%	0.27%	0.02%	0.00%	0.00%	1.12%	0.54%	0.07%	0.27%	0.00%
jesd204_tx (zcu102_ddr4_daq2_jesd204_tx_0)	0.72%	0.30%	0.01%	0.01%	<0.01%	1.27%	0.70%	0.03%	0.30%	0.00%
jesd204_rx (zcu102_ddr4_daq2_jesd204_rx_0)	0.92%	0.53%	0.22%	0.02%	0.02%	1.58%	0.86%	0.11%	0.53%	0.00%
jesd204_phy (zcu102_ddr4_daq2_jesd204_phy_0)	1.04%	0.70%	0.43%	<0.01%	<0.01%	1.99%	1.04%	0.00%	0.70%	0.00%
ila_0 (zcu102_ddr4_daq2_ila_0_0)	0.76%	0.59%	0.15%	0.06%	0.04%	2.05%	0.60%	0.30%	0.59%	14.31%
gnd_cell (zcu102_ddr4_daq2_gnd_cell_0)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
global_reset_0 (zcu102_ddr4_daq2_global_reset_0_0)	<0.01%	<0.01%	0.00%	0.00%	0.00%	<0.01%	<0.01%	0.00%	<0.01%	0.00%
dma_rst (zcu102_ddr4_daq2_dma_rst_0)	<0.01%	<0.01%	0.00%	0.00%	0.00%	0.02%	<0.01%	<0.01%	<0.01%	0.00%
dma_interconnect (zcu102_ddr4_daq2_dma_interconnect_0)	0.12%	0.16%	0.00%	0.00%	0.00%	0.39%	0.07%	0.10%	0.16%	0.00%
dma_controller_0 (zcu102_ddr4_daq2_dma_controller_0_0)	0.70%	0.47%	0.11%	0.00%	0.00%	1.51%	0.67%	0.06%	0.47%	6.91%
dma_axis_register (zcu102_ddr4_daq2_dma_axis_register_0)	0.01%	0.02%	0.00%	0.00%	0.00%	0.07%	0.01%	0.00%	0.02%	0.00%
ddr4_interconnect (zcu102_ddr4_daq2_ddr4_interconnect_0)	0.36%	0.18%	0.00%	0.00%	0.00%	0.74%	0.35%	<0.01%	0.18%	0.00%
ddr4_axi_rst (zcu102_ddr4_daq2_ddr4_axi_rst_0)	<0.01%	<0.01%	0.00%	0.00%	0.00%	0.03%	<0.01%	<0.01%	<0.01%	0.00%
ddr4_0 (zcu102_ddr4_daq2_ddr4_0_0)	3.35%	1.96%	0.17%	0.12%	0.00%	6.30%	3.15%	0.38%	1.96%	2.80%
axis_channel_select_t_1 (zcu102_ddr4_daq2_axis_channel_select_t_1_0)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
axis_channel_select_t_0 (zcu102_ddr4_daq2_axis_channel_select_t_0_0)	<0.01%	0.03%	0.01%	0.00%	0.00%	0.08%	<0.01%	0.00%	0.03%	0.00%
axis_channel_select (zcu102_ddr4_daq2_axis_channel_select_0)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
Window_Function (Window_Function_imp_1PL9JI4)	0.05%	0.08%	0.04%	0.00%	0.00%	0.28%	0.05%	<0.01%	0.08%	0.44%
GAKA_ch_0 (GAKA_ch_0_imp_W4B1O3)	0.38%	0.25%	0.13%	0.00%	0.00%	0.88%	0.32%	0.13%	0.25%	0.00%
DecimSerial (DecimSerial_imp_1M282CU)	0.13%	0.10%	0.15%	0.00%	0.00%	0.45%	0.13%	0.00%	0.10%	0.00%
DDC_Chain (DDC_Chain_imp_BSP809)	2.62%	2.30%	1.67%	0.00%	0.00%	4.06%	2.04%	1.11%	2.30%	0.88%
Clock_Hardware (Clock_Hardware_imp_1KEE3UO)	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
ADC_Input (ADC_Input_imp_1QQP8XY)	0.00%	<0.01%	0.00%	0.00%	0.00%	0.03%	0.00%	0.00%	<0.01%	0.00%
i_daq2_spi (daq2_spi)	<0.01%	<0.01%	0.00%	0.00%	0.00%	<0.01%	<0.01%	0.00%	<0.01%	0.00%
dbg_hub (dbg_hub)	0.18%	0.13%	0.02%	0.00%	0.00%	0.46%	0.16%	0.02%	0.13%	0.00%
inst (xsdbm_v3_0_0_xsdbm)	0.18%	0.13%	0.02%	0.00%	0.00%	0.46%	0.16%	0.02%	0.13%	0.00%

Back Up – Status of work

Publication and Thesis

- A first paper is under work,
- This work was presented (apart from HIRSAP meetings) in: **KRYO 2019**, **DTS 2021** and **KSETA Workshop 2022**,
- Also contributing to other works publications: Juan Manuel Geria and Manuel García Redondo,
- Sketch proposal for the **thesis**, (~10% written).

Deadlines and Credits

- The total credits for UNSAM side are complete: 20 credits in courses,
- CONICETs stipend is available until April 2024,
- UNSAM PhD was started in April 2018,
- KIT PhD was started in 2019.

Back Up – Moon Scan