Requirements and Block Diagram of SiPM Readout ASIC for ANDES

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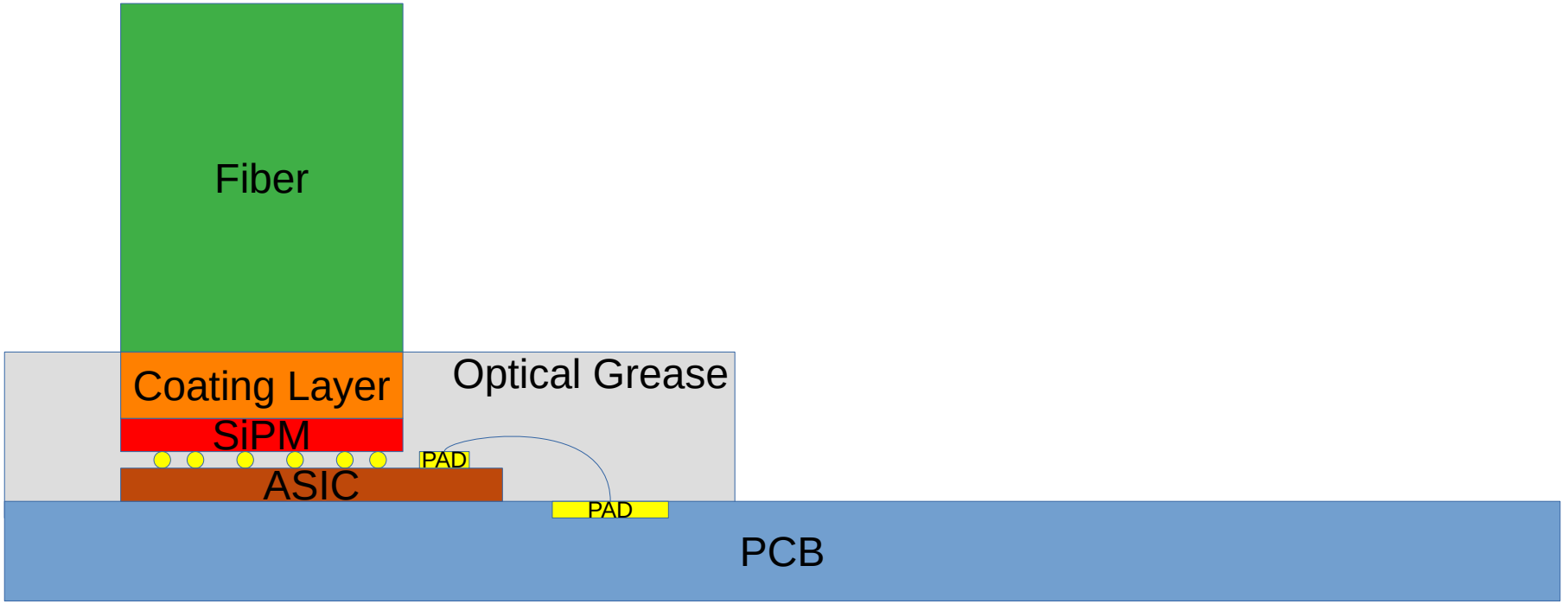
Requirements

- Every Muon must be detected
- Detection of every incoming photon with <100 ps rms time resolution within an event
- Event = muon generating several photons
- Event rate is very low
  - However several photons will arrive in very short time

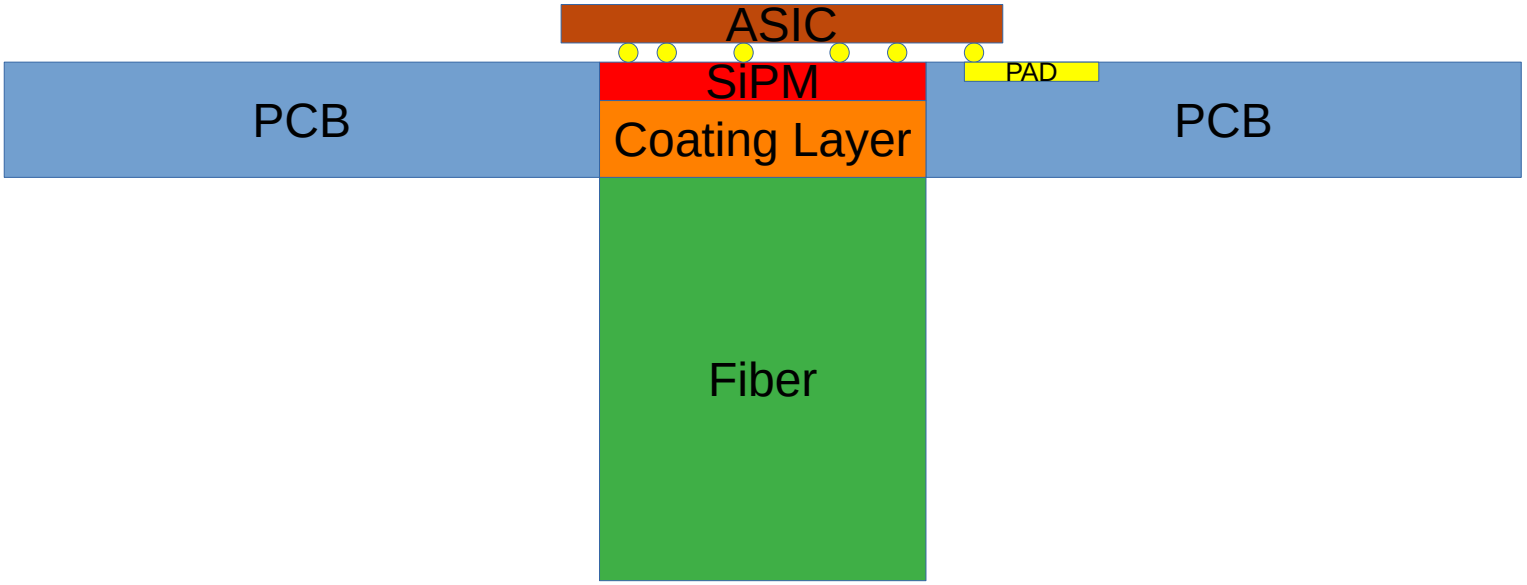
Requirements

- One Fiber will be connected to one SiPM + ASIC to have modular system
- ASIC and SiPM must have circular active area with diameter of 1.2 um
  - Proposed 1.3 um * 1.3 um considering tolerances??
- SiPM must be bump-bonded to ASIC
- ASIC must be wire bonded to PCB
  - Unfortunately TSV option for IHP is only possible to create ground plane and not for PADs
  - How to do coupling to fiber? Housing around SiPM??
  - Is it possible to flip ASIC+SiPM and make hole in PCB → Bumb-bond ASIC to PCB

Idea of SiPM to PCB Connection by Wire-bonding



Idea of SiPM to PCB Connection by bump-bonding



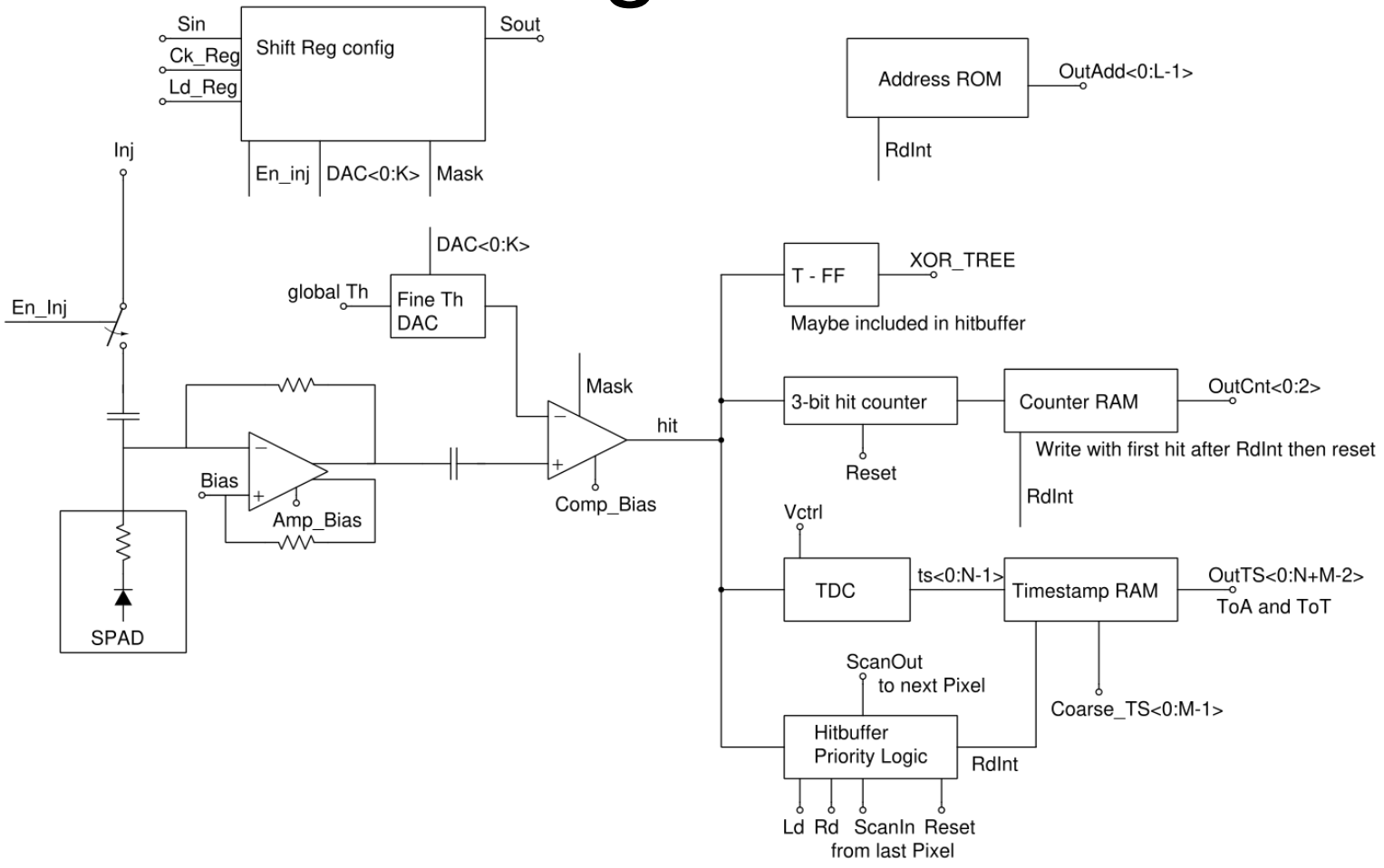
Activities to Improve Knowledge of Specification

- Tests with Muon Telescope at IteDA
  - Determine photon amount and arrival time distribution from different positions in the scintillator bar by AMIGA-SiPM + Amplifier + Oscilloscope
- Understand how this measurement can be improved by higher time resolution and angle detection

Functionalities of one Channel

- One Channel will be connected to one SPAD + quenching Resistor
- It has to provide:
  - Bias for the SPAD
  - Comparator for generating digital hit generation
    - Hit happens when SPAD fires due to incoming photon
  - Threshold tuning of the Comparator Threshold
  - Assign precise timestamp of time of arrival (ToA) and time over threshold (ToT) of hit signal
  - Reset function for triggered readout

Block Diagram of Pixel



Blocks of Pixel

- Bias DAC for SPAD
- Amplifier if needed
- Comparator
- Threshold Tuning DAC
- TDC + RAM for ToA and ToT
- Hitbuffer to manage readout and zero supression
- Counter to count hits that appear between first hit and readout
- Address ROM
- Connection to XOR Tree for global counter or other proposal to generate self trigger here????

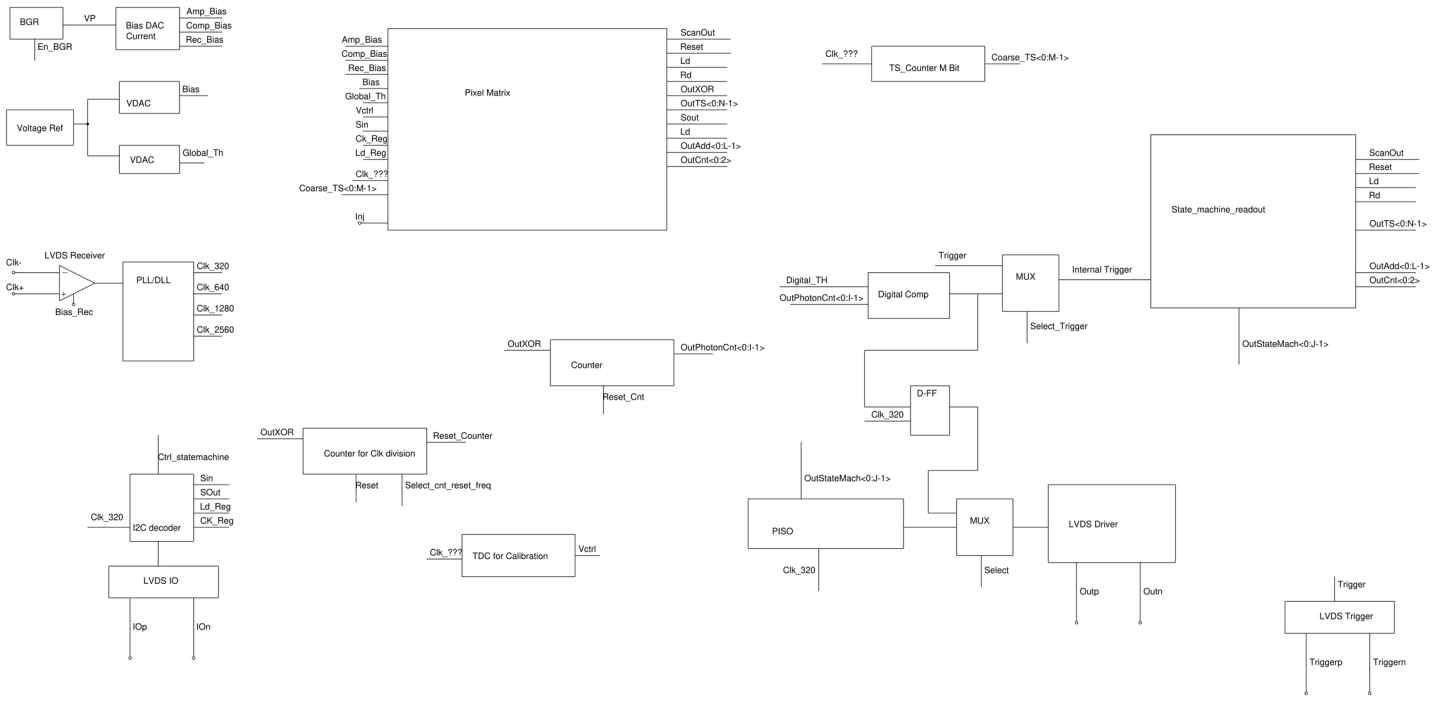
Functionalities of ASIC

- Temperature Sensor
- Current or voltage reference
- I2C slow control interface
- Availability of triggered and untriggered readout
- Self Triggering to reduce data-rate for dark counts
- Triggered Readout for complete array of ASICs → ability of saving triggered data before readout

Functionalities of ASIC

- Control voltage DLL/PLL can act as temperature sensor
- Timestamp data can be stored in Pixel memory (DRAM) until reset to be available for trigger
  - Then we just have to do regular resets

Block Diagram of Pixel



Blocks of ASIC

- Bandgap Reference for Refrence Current of Voltage
- Current DACs to bias amplifiers
- Global Coarse DACs for Threshold and Bias
- PLL/DLL to generate chip clock
- I2C and shift Register for slow control
- LVDS-Drivers
- Statemachine to manage readout
- PISO for readout
- Global counter for self triggering → Digital comparison to digital threshold to generate trigger