

Advancing front-end readout ASICs with BiCMOS SiGe technology for ultra-fast sensors

PhD Thesis Proposal

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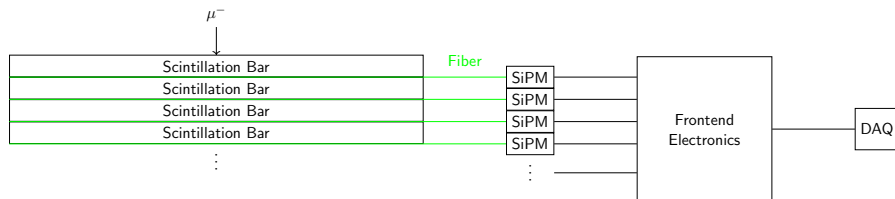


Universidad Nacional
de San Martín



Muon Detection

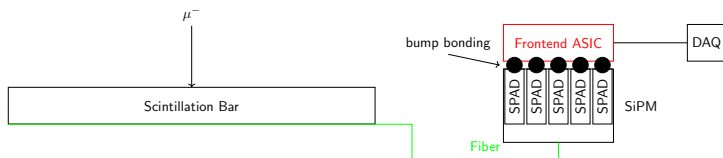
- Aim: Improve muon detection in AMIGA [1] and ANDES [2] experiments



Schematic of Current AMIGA Muon Detection Setup [3], [4]

- One SiPM per scintillation bar
 - connected to one readout channel in frontend
- Time resolution only by counting incoming photons in a certain time interval

Proposed Muon Detection Setup



Proposed Detector for one Scintillation Bar in ANDES

- High-granularity SiPM¹ of FBK[5] using 2D integration technology
 - reduced optical cross-talk due to trench isolation
 - pile-up mitigation
- SiPM bump-bonded to frontend ASIC
- Readout with high time resolution and high granularity
 - detection of angle of incoming photon and fiber delay

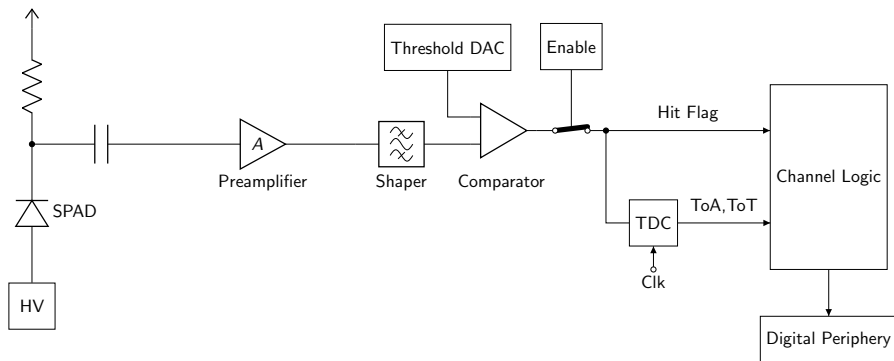
→ improved muon hit position resolution

¹joint development between KIT-IPE and FBK

Activities

- Design frontend readout ASIC for advanced SiPM technology
 - with high-granularity
 - each SPAD cell is readout individually
 - photon counting with very high time resolution
- Characterization of designed ASIC
 - testing general functionality
 - timing characterization
 - testing under bad environmental conditions
- High-density integration by bump bonding of SiPM to ASIC
 - using gold-stud bumping at KIT-IPE [6]
- Testing of hardware with muon counter at ITeDA

SPAD Readout



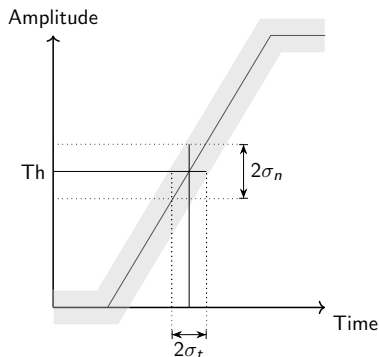
Proposed Readout Chain for one Pixel/SPAD

Time Resolution

Time jitter ¹

$$\sigma_t = \frac{\sigma_n}{\left. \frac{dV}{dt} \right|_{V_T}} \approx \frac{t_r}{S/N}$$

- High time resolution requires
 - Fast rise time
 - High signal to noise ratio

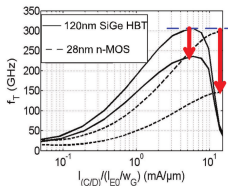


Threshold Crossing [7]

¹ $\sigma_n = \frac{S}{N}$, S: Signal amplitude, N: RMS-noise voltage

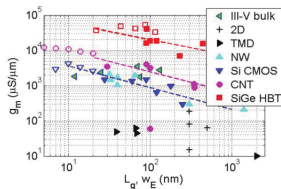
The solution: Heterojunction Bipolar Transistors (HBT)

- High time resolution requires
 - Fast Amplifiers = high f_T



Transit frequency f_T
HBT vs. MOSFET [8]

- Pixelated design requires
 - low area consumption



g_m vs. area of different
technologies [8]

- low noise

- low power consumption

→ HBT offers better performance in analog circuits than CMOS

SiGe BiCMOS

- SiGe HBT performance very good for analog design
- CMOS has advantages for
 - low-power digital design
 - bias circuits, because PMOS available

→ SiGe BiCMOS

- Our process: IHP SG13G2 130 nm SiGe BiCMOS with $f_T = 300$ GHz [9]
 - IHP is a research institute working closely together with KIT
 - IHP offers the HBTs with highest f_T
 - PDK for Cadence Virtuoso design environment
 - already used for pixel sensors with high time resolution[10]



Summary

- New generation of SiPM for muon counters in AMIGA and ANDES experiments
 - SiGe BiCMOS technology allows SiPM readout with
 - high granularity
 - high time resolution
- ASIC development for measurements with high spatial and time resolution

Bibliography I

- [1] AMIGA, [Online]. Available: <https://www.auger.org/observatory/amiga>.
- [2] ANDES, [Online]. Available: <https://andeslab.org/>.
- [3] A. Aab, P. Abreu, M. Aglietta, *et al.*, “Muon counting using silicon photomultipliers in the AMIGA detector of the pierre auger observatory,” *Journal of Instrumentation*, vol. 12, no. 03, P03002–P03002, Mar. 2017. DOI: [10.1088/1748-0221/12/03/p03002](https://doi.org/10.1088/1748-0221/12/03/p03002). [Online]. Available: <https://doi.org/10.1088/1748-0221/12/03/p03002>.

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- [6] M. Caselle, T. Blank, F. Colombo, *et al.*, “Low-cost bump-bonding processes for high energy physics pixel detectors,” *Journal of Instrumentation*, vol. 11, no. 01, pp. C01050–C01050, Jan. 2016. DOI: 10.1088/1748-0221/11/01/c01050. [Online]. Available: <https://doi.org/10.1088/1748-0221/11/01/c01050>.
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- [8] N. Rinaldi and M. Schröter, *Silicon-Germanium Heterojunction Bipolar Transistors for mm-Wave Systems: Technology, Modeling and Circuit Applications* -. Aalborg: River Publishers, 2018, ISBN: 978-8-793-51961-9. DOI: 10.13052/rp-9788793519602.

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- [10] L. Paolozzi, “Design of sige bicmos monolithic pixel sensors with picosecond-level time resolution,” (2019), [Online]. Available: https://indico.fnal.gov/event/22290/contributions/66878/attachments/42092/50885/2019_12_06_Fermilab_cut.pdf (visited on 11/02/2021).

Logos:

IHP: <https://www.ihp-microelectronics.com/>

Back-up

Cadence Virtuoso

The image displays three overlapping windows from the Cadence Virtuoso suite:

- Schematic Editor:** Shows a circuit schematic for a pixel. The netlist on the left includes components like AmpOut, Emittor, EnInj, EnInjB, gnda, Inj, and readout. The schematic shows a differential pair of transistors with various biasing and feedback elements.
- Layout Suite:** Shows the physical layout of the circuit, including the substrate drawing and various layers (Substrate, Active, Metal, etc.).
- Visualization & Analysis XL:** Displays a transient response plot for the signal $V(T^+)$ /Amp.. The plot shows a sharp negative-going spike followed by a recovery to a steady-state level. The x-axis is time in nanoseconds (ns) from 0.0 to 260.0, and the y-axis is voltage in millivolts (mV) from -90.0 to 15.0.

Below the plots, the Design Variables and Analysis windows are visible:

Name	Value
rvddsa	150f
rvddsb	5
Vth_global	975m
Cdet	200f
vddsa	1.2
vccasc	1.2
vccs	1.2
BL	1

Type	Enable	Arguments
dc	<input checked="" type="checkbox"/>	t
noise	<input checked="" type="checkbox"/>	10 100G Automatic Start Stop /AmpOutAC/gnda/
tran	<input checked="" type="checkbox"/>	0 250n conservative

Name/Signal/Expr	Value	Plot	Save	Save Options
Emittor		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Amplitude_AmpOutAC		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
rmsNoise		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>